Effect of bias variation on total uncertainty of CD measurements

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ABSTRACT

Measurement precision to process tolerance ratio (P/T) is an essential indicator of metrology readiness for a specific technology. A smaller ratio improves the process control achievable with a given metrology. The International Technology Roadmap for Semiconductors is calling for P/T ≤ 0.2. The "precision" (P) represents total uncertainty of the measurement. In practice P is estimated as the total variation of measurements made on a reference sample(s) over an extended period of time. This procedure leaves sample-to-sample variation of measurement bias outside of P (measurement bias is the difference between reported average and true value). We report on sample-to-sample CD SEM bias variation as characterized by CD AFM. CD AFM is virtually immune to material, layout and line profile variations and, therefore, is expected to have negligible sample-to-sample bias variation. We found that sample-to-sample CD SEM measurement bias variation (full range up to 15 nm) is often comparable to or even exceeds CD SEM reproducibility (full range of ~ 3 nm). Therefore, the current methodology of the "precision" measurement is leaving a significant component of the total measurement uncertainty unaccounted. The sample-to-sample bias variation (σ_B) measured on a set of samples representative to the specific technology needs to be corrected or added to the tool reproducibility (σ_R) in order to estimate total uncertainty of measurement (σ_P): $\sigma_P^2 = \sigma_B^2 + \sigma_R^2$. This may noticeably change the "precision" of CD SEM ($3\sigma_P$) and move P/T for the current 130 nm and 100 nm technologies well over the limit of 0.2. Should the industry keep CD SEM as a major in-line CD across chip metrology the sample-to-sample bias variation has to be significantly improved. Otherwise, chip manufacturers will likely fail to deliver required across chip gate CD uniformity.

Keywords: CD metrology, precision, P/T, measurement bias, line profile, CD SEM, CD AFM

1. INTRODUCTION

Development of current semiconductor technologies is demanding unprecedented control of critical dimensions (CD). According to the 2001 edition of International Technology Roadmap for Semiconductors (ITRS) in 2003 the industry is working on the 100 nm technology node which has a physical gate length of 45 nm [1]. The ITRS CD control guideline for isolated gates is 4.5 nm (3σ). In-line CD metrology is used to control gate CD. The smaller the total uncertainty of the measurement the better is the gate CD control. Often CD metrology is used to correct short-term process fluctuations as well as long-term trends. Therefore, for relatively stable process a bad metrology could be worse than no metrology at all. It is commonly accepted that P/T < 0.3 is needed for adequate process control [2,3]. The 2001 ITRS asks for P/T = 0.2 and as a result requests 0.9 nm (3σ) CD metrology precision for the 100 nm technology.

The total uncertainty of measurements (or "P" in P/T ratio) is usually estimated as "reproducibility" of the measurements, where reproducibility is the total variability associated with measurements made on the same sample under different, but typical conditions [3]. As we will show in this paper this definition of "P" leaves a significant part of the total uncertainty of measurements unaccounted.

Two types of in-line CD metrology, scatterometry (SCD) and CD SEM, are commonly used today for gate control. SCD has an outstanding often better than ~ 0.6 nm (3σ) reproducibility [4]. However, SCD requires special ~ 50×50 μm^2 test structure for the measurements and, therefore, can not be used for across chip gate CD control of individual transistors. CD SEM is still the main metrology used to control across chip gate CD uniformity [5]. Reproducibility of CD SEM measurements has gradually improved over the years and for poly line CD measurements it stands today at about the 1.5 nm (3σ) level [6]. It is no doubt that CD SEM reproducibility will be improved even further. The major problem with the use of CD SEM for across chip gate CD control is a significant sample-to-sample variation of SEM measurement bias. The measurement bias is the difference between the average of measurements made on the same object and its true

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value. Constant sample-to-sample measurement bias affects accuracy of the measurement but does not affect gate CD control or the total uncertainty of the measurement "P". Variable sample-to-sample measurement bias affects accuracy and the total uncertainty of the measurement (Fig. 1). In the past variation of measurement bias was much less than reproducibility and, therefore, this portion of the total CD SEM measurement uncertainty was simply ignored. Now when CD SEM reproducibility has reached 1.5 nm the sample-to-sample bias variation becomes comparable or even dominating component of the total uncertainty of SEM measurements.

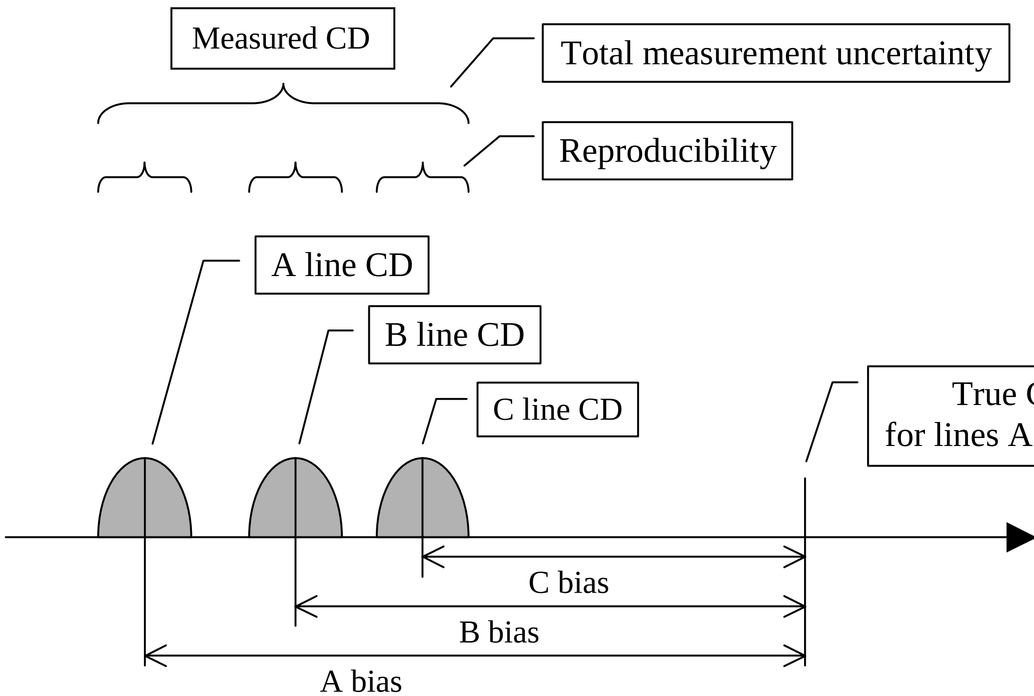

Fig. 1. Illustration of the sample-to-sample bias variation and its influence on the total uncertainty of the measurement.

This paper illustrates the dependence of CD SEM bias variation on some line parameters such as height and sidewall angle, as well as on proximity of the line to another line (pitch) and to the shallow trench isolation (STI). Because of this complexity of the phenomenon sample-to-sample CD SEM bias variation has to be defined on a set of samples representative to the specific technology (pre-calibrated CD standards, should they exist, cannot be used). How one can get true CD values for the representative set of samples? One possible approach is to do CD SEM measurements followed by transmission electron microscopy (TEM). However, taking into account huge volume of samples needed for such evaluation we think this approach is non-practical. We found that CD AFM is well suited for sample-to-sample CD SEM bias variation evaluation. CD AFM measurement bias is virtually material, line profile and layout independent. Therefore, CD AFM measurements should have insignificant bias variation. Fig. 2 shows short-term dynamic repeatability of ~ 1.7 nm (3σ) observed on average for CD AFM measurements of 4 polysilicon lines. CD AFM dynamic repeatability is comparable with CD SEM reproducibility and hence should be sufficient for evaluation of sample-to-sample CD SEM bias variation.

This paper summarizes observations made over several years on materials representing several technology nodes. In-line CD SEM tools of 3 different advanced models have been used to collect the data. The patterning process and tool brand information is proprietary and hence will be intentionally omitted.

2. ORIGIN OF SEM SAMPLE-TO-SAMPLE BIAS VARIATION

The mechanism of CD SEM sample-to-sample bias variation is well understood [7, 8]. Modern in-line CD SEM tools use various empirical edge criteria to extract line CD from measured secondary electron signal of the line. According to Postek and Vladár [7] only 10% of the signal is related to secondary electrons coming directly from the object of interest. The remaining 90% of the secondary electron signal is generated with participation of the high-energy backscattered electrons in some vicinity of the line or even far from the sample at internal instrument components. Theoretically, various factors related to the sample composition and geometry could affect secondary electron collection efficiency and, therefore, the exact SEM waveform of the line and SEM bias. Noticeable effect of sidewall angle on CD SEM bias was modeled and reported by Villarrubia et. al. [8]. One may speculate that many other factors such as line material, height, profile, edge roughness, sample topography and layout in vicinity of the line could affect the bias. The following results should help to quantify some of these effects.

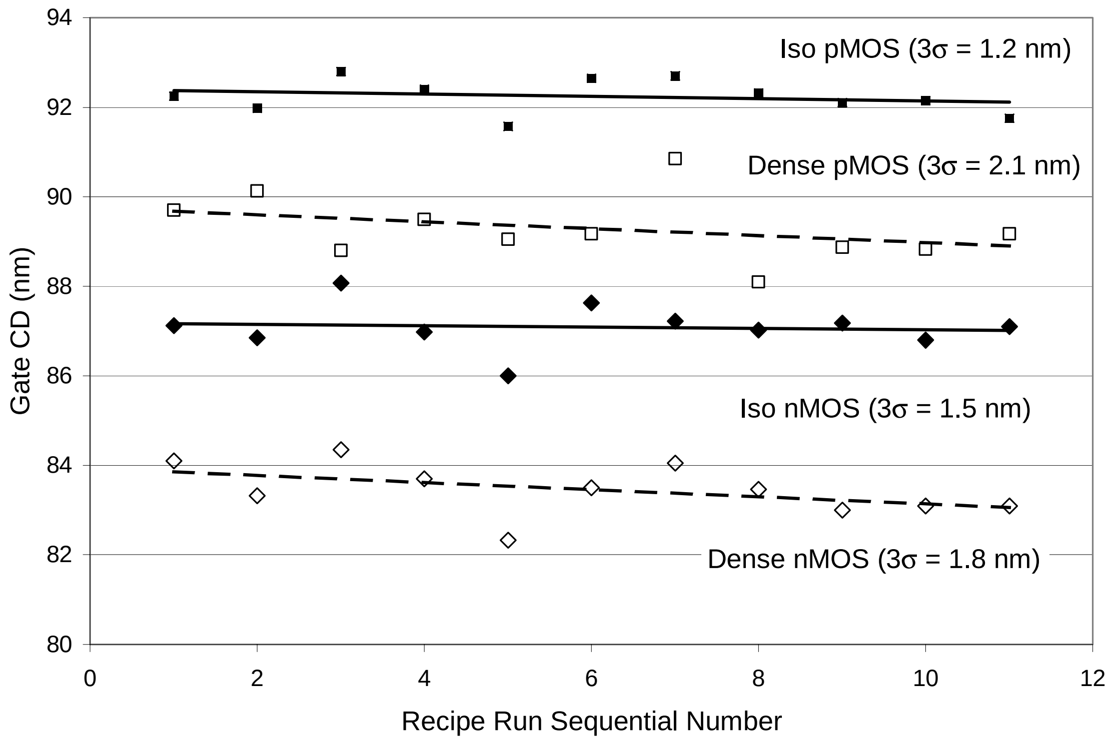

Fig. 2. Short-term dynamic repeatability of CD AFM measurements obtained on isolated and dense polysilicon gates.

3. EXPERIMENTAL

CD SEM measurements were performed on several advanced in-line tools of different brands and generations. The absolute value of the CD SEM bias can be affected by specifics of the tool geometry and design and, therefore, is not important. CD SEM bias was defined against line CD measured by CD AFM at 10% of the line height. CD AFM was done using Veeco's SXM-320. The CD mode of AFM operation is designed to provide accurate measurements of critical dimensions and 2D profiles of lines and trenches.

Fig. 3 illustrates the dependence of CD SEM bias on sidewall angle. The poly gate CD measurements were done on transistors of two types: (a) narrow source and drain (the gate is close to STI) and (b) wide source and drain (the gate is far from STI). Both types of transistors demonstrate the same trend - the larger the sidewall angle the higher is the SEM bias. The slope of the trend is ~ 2 nm of the bias variation per degree of the line sidewall angle. On average gates of the "wide" transistors appear 3 nm larger than similar gates of the "narrow" transistors. Therefore, STI proximity to poly line does noticeably affect CD SEM bias. Should CD SEM be used as a metrology tool for proximity correction the "wide" transistor gate CD will be incorrectly adjusted by 3 nm to match gate CD of the "narrow" transistors.

Fig. 4 confirms this STI proximity effect on CD SEM bias. This time SEM bias offset of ~ 4.3 nm (c.f. 3 nm) was observed for gate CD of the "wide" and "narrow" transistors. Interestingly enough this wide-to-narrow bias offset changes with edge definition criteria. Higher bias offset (up to 13 nm) was observed for the lower first derivative threshold (Fig. 4). Apparently STI proximity has larger effect on the tails of the poly line waveform.

Fig. 5 shows probably the most drastic case of sample-to-sample CD SEM bias variation. SEM bias variation as high as 15 nm has been detected. These data represent measurements done on periodic structures of ~ 100 nm polysilicon lines placed at various pitches. The line orientation on the wafer "vertical" vs. "horizontal" apparently affects SEM bias as well. Through pitch optical proximity correction (OPC) is a very common line CD adjustment used by every chip manufacturer. CD SEM is currently used for the input data collection for the OPC models. Should the SEM data presented in Fig. 5 be used as an OPC model input the physical dimensions of the line through pitch will vary as much as (10-15) nm. The real danger of the situation is that no problem would be detected if the same SEM is used to monitor the quality of the OPC. Therefore, the problem will become evident only at later stage of the process development when electrical data are available to trace across chip CD non-uniformity.

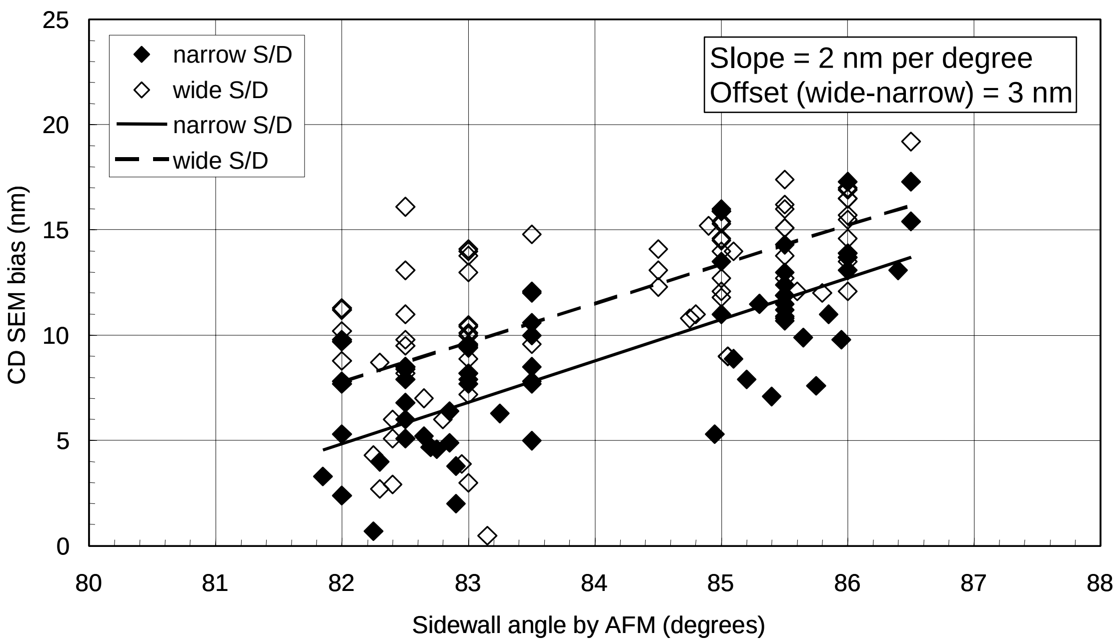

Fig. 3. Sample-to-sample CD SEM bias dependence on polysilicon line sidewall angle. The "narrow" and "wide" source and drain transistor cases stand for less than 0.5 µm and more than 1 µm proximity of the line to STI, respectively. CD SEM bias is defined as a difference between mid-derivative line CD by SEM and CD by AFM at 10% of the line height. Sidewall angle is measured by AFM.

The through pitch CD SEM bias variation may vary significantly depending on a variety of factors: SEM tool used, line material (photoresist vs. hardmask vs. polysilicon), line height, profile, etc. Therefore, the bias dependence has to be defined for each technology and even for each substantial modification of the patterning process within the technology. Fig. 6 represents through pitch SEM bias variation for polysilicon lines processed with a different patterning sequence. Bias variation of less than 4 nm was observed. The line height is the major difference between polysilicon lines measured in these 2 cases (c.f. Figs. 5 and 6).

4. DISCUSSION

Figs. 3-6 illustrate significant, up to 15 nm, sample-to-sample CD SEM bias variation. This measurement uncertainty vastly exceeds the total uncertainty of 1.8 nm (6σ) requested by the ITRS for in-line CD metrology for the 100 nm technology node. More than that it noticeably exceeds the total range of process control of 9.0 nm (6σ) for the same technology. The sample-to-sample bias variation is a major component of the total uncertainty of CD SEM measurements and has to be properly characterized and added to the total tool precision or corrected. The challenge is to devise a commonly accepted and robust procedure to measure the sample-to-sample CD SEM bias variation. The issue must be resolved if CD SEM is to continue its major role as the in-line metrology of choice for across chip CD control. Otherwise, chip manufacturers will very likely fail to deliver required across chip gate CD uniformity.

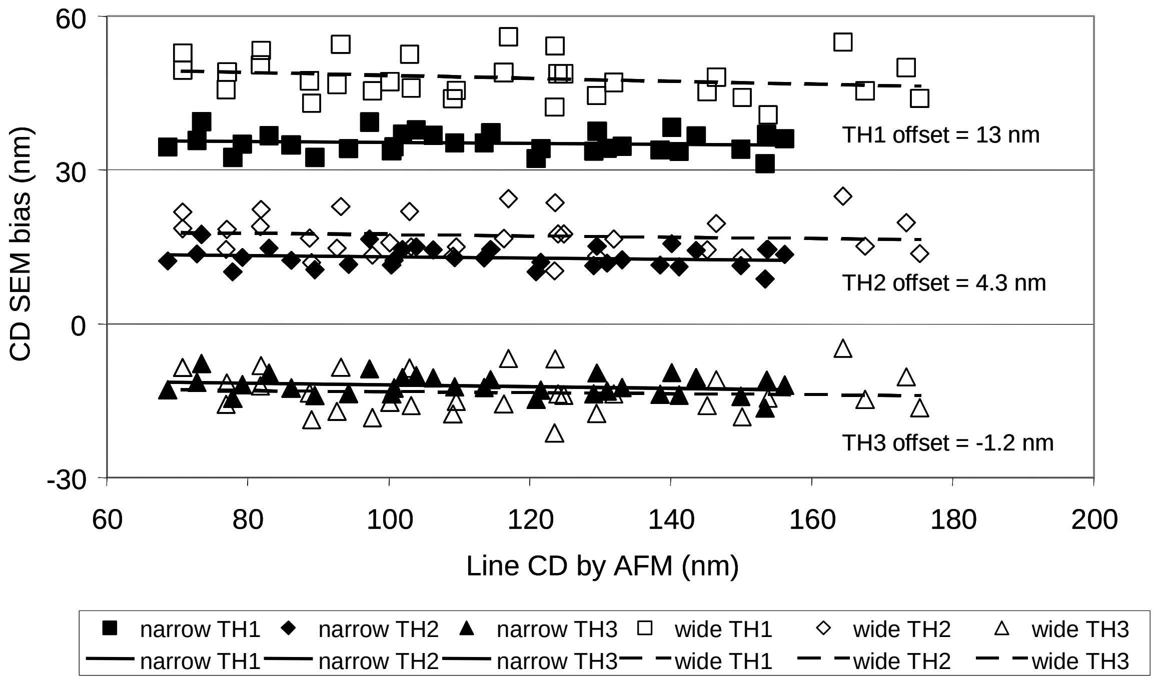

Fig. 4. Sample-to-sample CD SEM bias dependence on polysilicon line CD. The “narrow” and “wide” source and drain transistor cases stand for less than 0.5 μm and more than 1 μm proximity of the line to STI, respectively. Data for 3 different line edge definition criteria are shown. TH1 < TH2 < TH3 are the first derivative thresholds used to extract line CD from SEM waveform of the line. CD SEM bias is defined as a difference between mid-derivative line CD by SEM and CD by AFM at 10% of the line height.

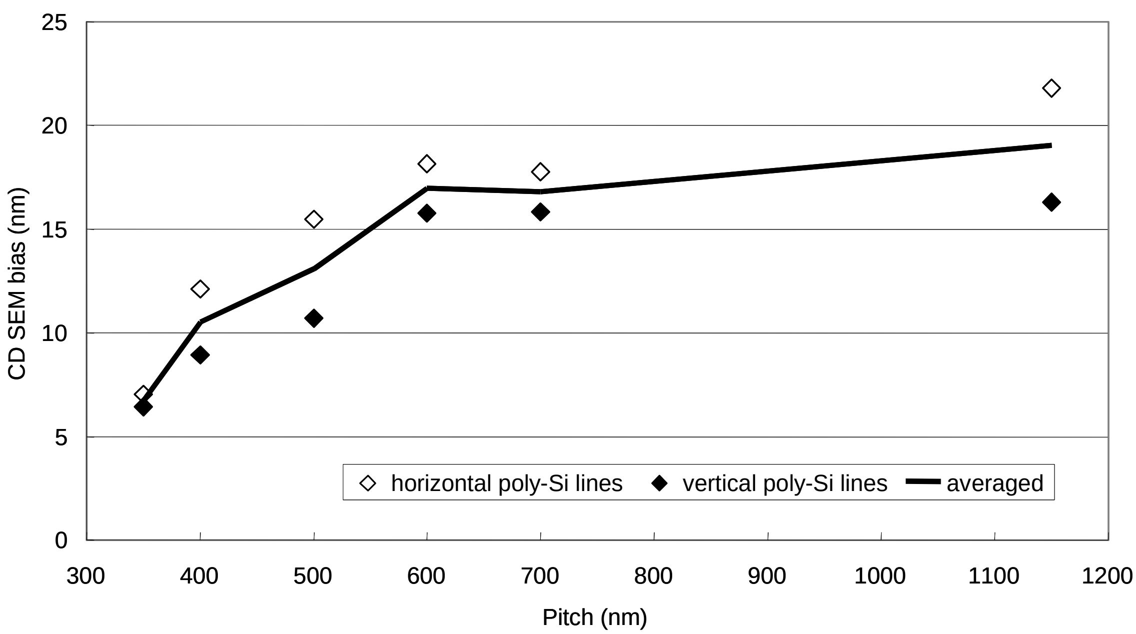

Fig. 5. Sample-to-sample CD SEM bias dependence on polysilicon line pitch. Lines of 2 different orientations on wafer “horizontal” and “vertical” were measured. CD SEM bias is defined as a difference between mid-derivative line CD by SEM and CD by AFM at 10% of the line height.

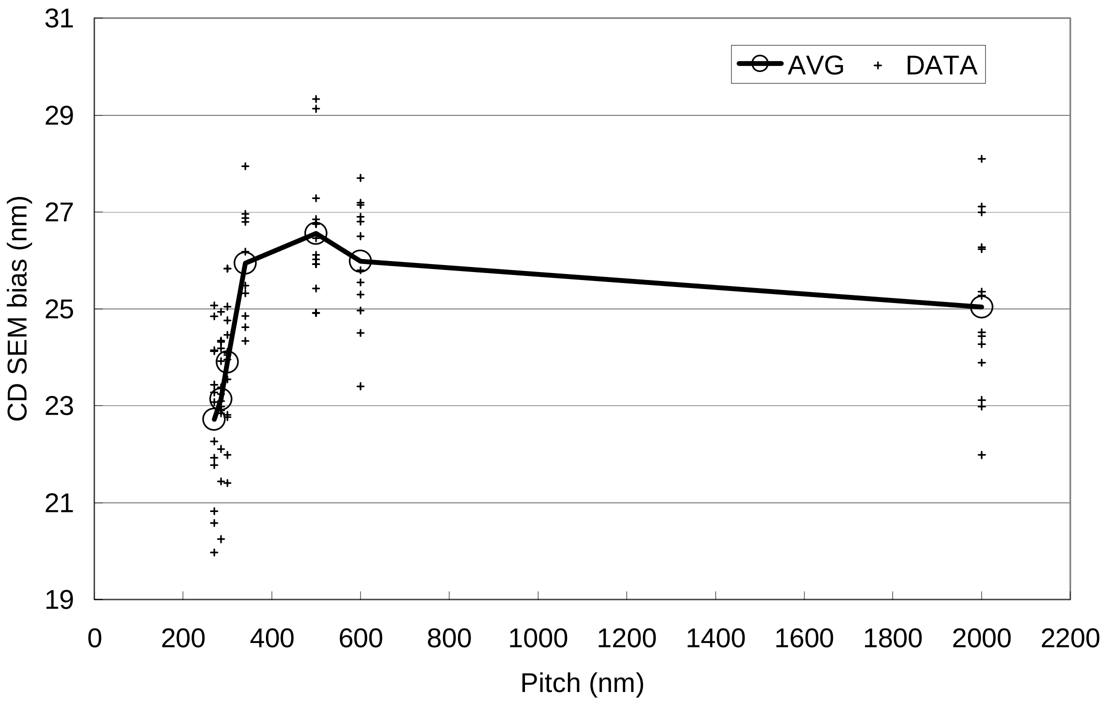

Fig. 6. Sample-to-sample CD SEM bias dependence on polysilicon line pitch. The measured polysilicon lines had smaller height and were patterned using different process compare to the case reported in Fig. 5. CD SEM bias is defined as a difference between mid-derivative line CD by SEM and CD by AFM at 10% of the line height.

Today improvement of the sample-to-sample bias variation is not motivated simply because this critical element of CD metrology tool performance is not monitored. The correct SEM design, which will minimize the bias variation, has to be distinguished and rewarded. Therefore, sample-to-sample bias variation measurements must become a part of routine SEM tool evaluation and benchmarking.

5. CONCLUSION

Measurement precision to process tolerance ratio (P/T) is an essential indicator of metrology readiness for a specific technology. The “precision” (P) represents total uncertainty of the measurement. In practice P is estimated as the total variation of measurements made on a reference sample(s) over extended period of time. This procedure leaves sample-to-sample variation of measurement bias outside of P. Using CD AFM as a reference tool we found that sample-to-sample CD SEM measurement bias variation can be as high as 15 nm and is often comparable or even exceeds CD SEM reproducibility. Therefore, the current methodology for the “precision” measurement [3] is leaving a significant component of the total measurement uncertainty unaccounted. The sample-to-sample bias variation (σ_B) measured on a set of samples representative to the specific technology needs to be properly corrected or added to the tool reproducibility (σ_R) in order to correctly estimate total uncertainty of measurement (σ_P): $\sigma_P^2 = \sigma_B^2 + \sigma_R^2$. This may noticeably change the “precision” of CD SEM ($3\sigma_P$) and move P/T for the current 130 nm and 100 nm technologies well over the limit of 0.2. The issue must be resolved if CD SEM is to continue its major role as the in-line metrology of choice for across chip CD control. Otherwise, chip manufacturers will likely fail to deliver required across chip gate CD uniformity.

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