The role of AFM in semiconductor technology development: the 65 nm technology node and beyond.

Vladimir A. Ukraintsev, Christopher Baum, Gary Zhang and Craig L. Hall
Silicon Technology Development, Texas Instruments Inc., Dallas, TX, 75265, USA

ABSTRACT

The International Technology Roadmap for Semiconductors (ITRS) predicts that atomic force microscopy (AFM) will become an in-line metrology tool starting at the 65 nm technology node. Others argue that AFM is not suitable beyond the 65 nm node due to probe size limitations [1]. This presentation examines the current state of AFM in semiconductor technology development and manufacturing. The following AFM applications are reviewed: post chemical mechanical polishing (post-CMP) and post reactive ion etching (post-RIE) topography measurements, critical dimension (CD) scanning electron microscopy (SEM) and optical scatterometry (OCD) calibration and long-term accuracy monitoring, across integrated circuit (IC) CD bias measurements (OCD lines vs. real circuit), optical proximity correction (OPC) modeling verification, non-destructive 3D metrology (resist, gate, sidewall offsets, holes and trenches). This current state is contrasted with upcoming requirements, benefits and limitations of metrology tools. The topics include the following: an application specific analysis of AFM limitations, the merits and limitations of transmission electron microscopy (TEM) as reference technique for AFM, CD SEM and OCD, the impact of sample-to-sample bias variation on total measurement uncertainty of TEM, CD SEM, OCD and AFM, the unique role of AFM in establishing across CD metrology correlation and accuracy, and need for a new type of intelligent in-line CD metrology tools, which would combine the merits of OCD, CD SEM and AFM.

Keywords: AFM, critical dimensions, CD, sample-to-sample bias variation, total measurement uncertainty

1. INTRODUCTION

Every semiconductor technology node brings new challenges for CD metrology. The last 3 deep sub-micron nodes (130, 90, and 65 nm) have changed CD metrology qualitatively. What are the new challenges of the deep sub-micron CD metrology? First of all, CD metrology underwent transition from one-dimensional to truly three-dimensional (3D) metrology. From CD metrology perspective, integrated circuit (IC) is not planar anymore. The transition to 2D metrology began near the 130 nm node when the transistor gate height-to-length aspect ratio exceeded critical value of unity. Simple estimation shows (Fig. 1) that for the gate with aspect ratio of 1:1 and sidewall angle (SWA) of 1 degree difference between the top and the bottom CD would exceed the whole measurement uncertainty budget for the 10% gate CD process tolerance and precision to tolerance ratio (P/T) of 0.2. Therefore, it became critical not only to measure the gate CD with needed precision, but also to know exactly at what height the CD was measured. Moreover, also in the 130 nm node, variation of CD along the gate width became comparable with the gate CD process tolerance. Two components of gate width variation can be distinguished. The random component of gate width variation is also known as line width roughness (LWR). The systematic component of gate width variation caused by optical proximity effects is getting noticeable once the third transistor dimension, the gate width [2], is entering the deep sub-micron range. Therefore, starting from the 130 nm node complete 3D CD metrology has become essential for the proper gate process control.

Another new feature of deep sub-micron CD metrology is the significant contribution of sample-to-sample bias variation to the total measurement uncertainty. Figure 2 is illustrating relations between measurement reproducibility (or precision as defined by [3]), sample-to-sample bias variation and total measurement uncertainty. Impact of the sample-to-sample bias variation on the total measurement uncertainty has been discussed in detail elsewhere [4]. It was shown that in some cases sample-to-sample bias variation might be comparable or even exceed precision of CD SEM. CD SEM is not the only metrology tool where total measurement uncertainty is affected by sample-to-sample bias variation. Very little is yet known about sample-to-sample bias variation of such techniques as cross-sectional SEM (XSEM), scatterometry (OCD), AFM, and TEM. We will return to this topic later in the paper.

CD variation includes various components: lot-to-lot, wafer-to-wafer, across wafer, across field or chip, optical proximity effects, etc. It is widely accepted that no single metrology can solve the complex task of monitoring and controlling all of these components. Today, cross-calibration of various techniques working together is a key element of successful CD metrology. The multi-technique approach and an increasing role of simulation in transistor design demands not only precise, but accurate CD metrology. Since calibration of a CD metrology tool is in most cases application specific, it is impossible to design the universal calibration standard which will fit all CD metrology tools and all possible applications. For example, calibration of CD SEM or OCD using poly-Si lines would not necessarily guarantee accuracy of resist line measurements. One possible solution to this problem is to use a reference tool with minimal sample-to-sample bias variation to calibrate a technology and application specific, representative set of calibration samples traceable to a single CD standard.

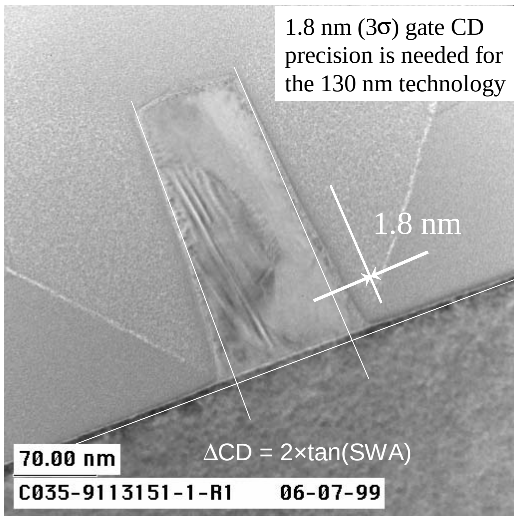

Figure 1. Comparison between 130 nm node gate CD precision and the top to bottom gate CD variation.

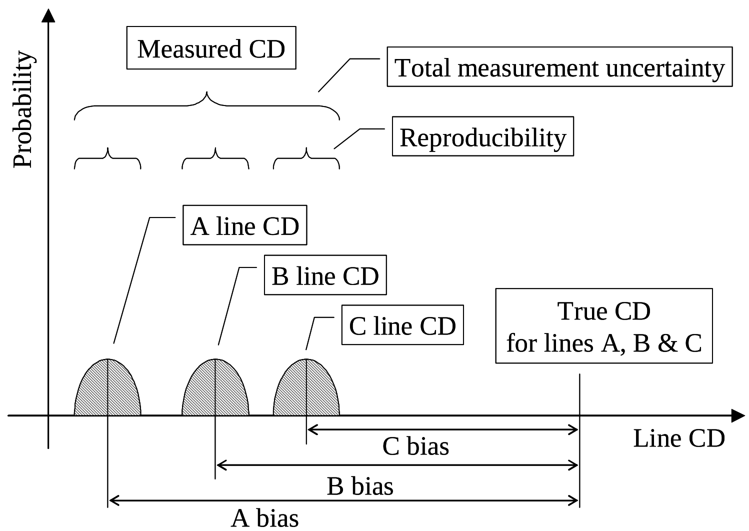

Figure 2. Relations between measurement reproducibility, sample-to-sample bias variation and TMU.

AFM holds a unique position in deep sub-micron CD metrology. AFM is the only non-destructive 3D metrology which does not need complex modeling to extract CD. It would be practically impossible to achieve and verify the required sub-nanometer measurement uncertainty of CD SEM and OCD without CD AFM. It is AFM's tolerance to material properties and layout proximity effects which makes AFM an ideal tool for sample-to-sample bias variation characterization. In absence of NIST traceable line CD standards, AFM has been successfully used by semiconductor companies as a reference tool for internal absolute calibration of other CD metrology tools. Recently CD AFM has been used by NIST to generate the first line CD standards [5].

It is the authors' opinion that AFM or other forms of scanning probe microscopy (SPM) will remain a valuable CD metrology tool for several semiconductor technologies to come, and possibly until transistors reach atomic dimensions. Of course to make this true many limitations of AFM must yet be resolved.

2. CD AFM TECHNIQUE

Conventional 1D and novel CD AFM have been described in detail elsewhere [6]. Only the basics of CD AFM and some details important for further discussion will be presented in this section. Two innovations made CD AFM possible: (1) vertical and lateral 2D atomic force sensing, and (2) special flared geometry probe. As Figure 3 illustrates, the 2D feedback, and the special probe's geometry guarantee that the left sidewall of the line is imaged by the right probe flare apex and the right sidewall is imaged by the left probe flare apex. This certainty makes line shape erosion unambiguous and CD extraction possible [6]. Measured line CD is simply a sum of the true line CD and the probe size. Once the probe size is known, the true line CD can be calculated.

Although many methods to measure the probe size exist, it is a real challenge to do this with the required nanometer accuracy. The best known method is to use a pre-calibrated artifact. Since a NIST traceable artifact is not yet available, most semiconductor (SC) companies have created their own internal CD standards. To verify calibration accuracy, one can use direct comparison between AFM and TEM data. The number of samples used for the cross calibration should be large enough to reduce measurement uncertainty (Fig. 4). TEM scale should be calibrated using NIST traceable samples.

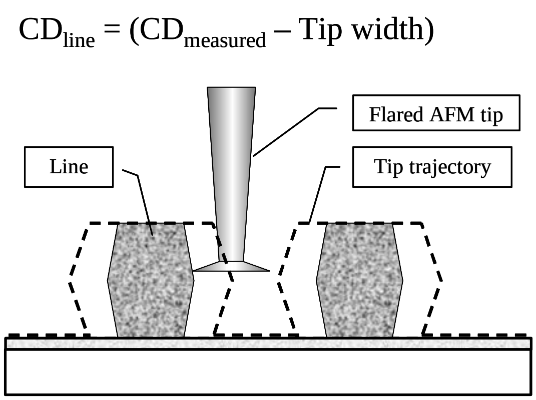

Figure 3. Illustration of CD AFM principle.

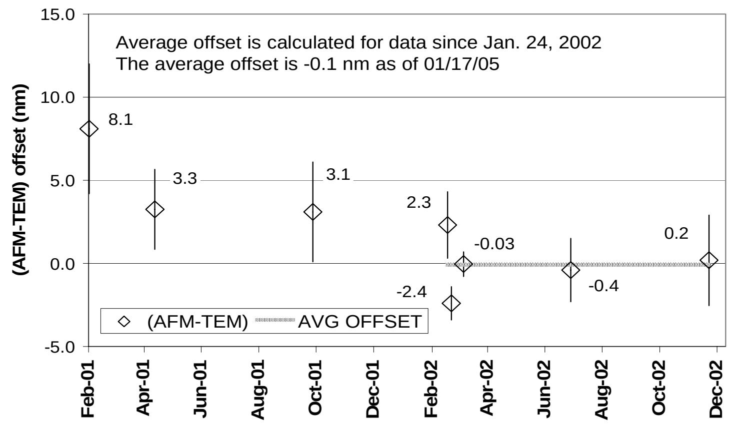

Figure 4. Many TEM images have been used to calibrate CD AFM.

Modern CD AFM tools are capable of sub-nanometer (3σ) precision (Fig. 5). The most important factors affecting CD AFM precision are probe contamination and wear. Therefore, CD AFM precision is sample dependent.

Resolution of CD AFM is often left out of discussion but deserves detailed consideration. An AFM probe is a 3D object and interacts with the sample in all 3 dimensions. Three basic types of probes are employed by CD AFM (Fig. 6). The “cylindrical” probes usually have less than 4 degrees total cone angle. The probe bottom diameter can be as small as 15 nm. The flared probes may have rounded or rectangular bottom. The smallest commercially available probes have ~ 50 nm bottom size in the fast scan direction (X). The rectangular probes are about 20-25% smaller in the slow scan direction (Y). The minimum specified flare is 5 nm. The flared probes are capable of imaging trenches with aspect ratio up to 7.

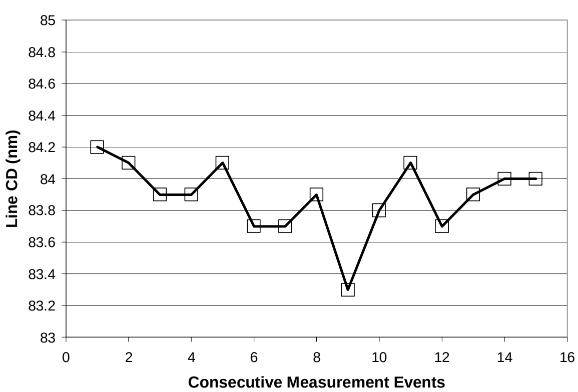

Figure 5. CD AFM dynamic repeatability of 0.7 nm (3σ) has been demonstrated for line CD measurements.

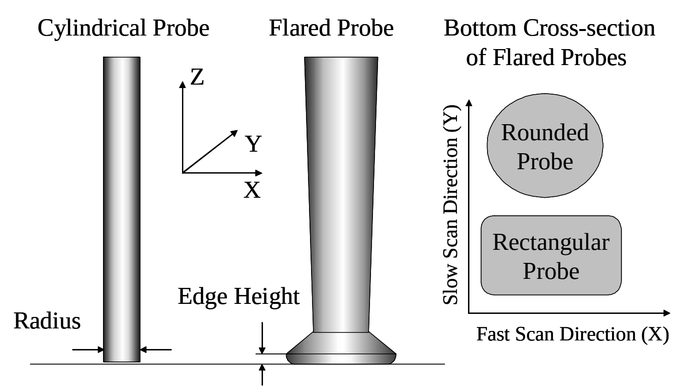

Figure 6. Types of probes used in CD AFM.

AFM resolution has two critical components: XZ and XY (Fig. 6). The XZ resolution is essential for line profiling and defined by the radius of curvature of the flare. Typical XZ resolution for fresh Si probe is about 10 nm. The resolution degrades with probe lifetime and usually causes the probe to be discarded after the resolution reaches a certain pre-specified limit. Since all modern CD AFM tools have YZ probe tilt of 2-3 degrees, the finite slow scan dimension of the probe may cause further degradation of XZ resolution. Therefore, the rounded probe may potentially offer better XZ or sidewall profile resolution. The most critical part of transistor gate profile is at its bottom. Because of the limited XZ resolution, CD AFM is virtually "blind" to the most important last 10 nm of the gate profile. This AFM limitation is to be discussed in detail later in the paper.

The XY resolution is essential for line sidewall roughness measurements. The maximum spatial frequency of line edge roughness (LER) or LWR measurements is limited by the slow scan dimension of the probe. The rectangular probe can be used to scan lines at 45 degrees (rather than at 90 degrees as in regular scan). In this case, the XY resolution will be limited by the radius of the curvature of the corner of the rectangular apex (Fig. 6). The radius of the corner is usually ~ 20 nm.

3. CURRENT APPLICATIONS OF AFM

In this section some representative examples of 1D and CD AFM application will be discussed with an accent on possible limitations for the future technology nodes. The following key applications of AFM are to be discussed: topography measurements in dense line-space areas, use of AFM as a reference CD metrology tool, and repeatable non-destructive CD measurements in 3D.

3.1. 1D AFM

AFM is used semiconductor (SC) industry wide for post-CMP topography and post-RIE depth controls [7]. AFM is also widely used for post-CMP and post thin film deposition roughness control, but those applications have been reviewed elsewhere [8] and are outside of the scope of this paper. The drivers for 1D AFM applications are increasing density of IC layouts and layout density dependent CMP and RIE macroloading effects. Considering tight across IC control, it is not enough anymore to characterize post-CMP topography or depth of RIE using large profilometry structures located in IC scribe. Figure 7 shows correlation between post-CMP shallow trench isolation (STI) topography measured at scribe structure using profilometry and topography measured by AFM in the middle of large SRAM array. As one can see the correlation is poor and the linear trend has slope far from unity. Therefore, CMP control based on scribe only metrology would lead to poor SRAM topography control.

SRAM arrays have the densest layout and are challenging even for AFM. Current AFM probe technology is offering cylindrical probes of 15 nm diameter. An interaction between the probe and trench sidewalls makes imaging unreliable once the trench size reaches ~ 30 nm. The cylindrical probes are lasting for thousands of sites while keeping required high XY resolution [9]. Conventional conical AFM probes deliver comparable (or even better) initial XY resolution but have much shorter and material dependent lifetime.

It is likely that better probe technology (smaller dimensions, task specific geometries, non-sticky materials, etc.) and smarter scan algorithms will keep AFM on top of topography tasks to the end of the ITRS.

3.2. CD AFM AS CD METROLOGY REFERENCE TOOL

This section covers 3 of the most important applications of CD AFM in SC technology development and manufacturing. Once again AFM is the only non-destructive 3D metrology which does not required modeling to extract CD. Measurement is virtually done by direct comparison of unknown CD to the reference sample or CD standard. AFM's main advantage as a reference tool is its tolerance to material properties and layout proximity effects. AFM probe-to-sample interaction is so localized that bias variation related to any proximity and material effects is expected to be well below one nanometer [10]. At the same time, sub-nanometer (3σ) precision can be achieved by CD AFM for most applications if data for several measurement sites is averaged. The sample size would depend on the particular application, but in most cases 5 to 10 samples should be enough to reach the required sub-nanometer precision. All of this makes CD AFM a unique reference tool with achievable sub-nanometer (3σ) total measurement uncertainty (TMU).

Table 1 is an attempt to estimate TMU for modern gate CD metrologies. The table summarizes observations by the authors, public domain data, and inputs from experts in various fields of CD metrology obtained through private communications. The values should be treated as estimates only and may very significantly depending on metrology tool and measurement methodology used.

The following components of the TMU have been considered: scale variation, dynamic repeatability, sample-to-sample bias variation and LWR. The estimate of TMU to gate CD tolerance (T) ratio is shown for 40 nm gate. As can be seen from the data the TMU/T ratio is poor even for OCD commonly used for gate CD process control. This explains why wafer average (rather than a single site) gate CD is often used for process control. Therefore, TMU/T ratio for wafer average gate CD has been estimated based on typical sample size used to estimate wafer average CD. Only random or site dependent components of TMU for wafer average (dynamic repeatability and LWR) will be affected by the sample size. The sample-to-sample bias variation components have been estimated based on multiple correlation studies conducted at Texas Instruments on the 65 nm technology node materials and modern AFM, SEM, and OCD tools. Some examples of these data will be presented in sections 3.2.1 and 3.2.2.

TABLE 1. Gate CD TMU for various CD metrologies and TMU/T ratios for the 65 nm technology node

	6σ Scale Accuracy (%)	6σ CD Repeatability (nm)	Bias Variation (nm)	6σ LWR (nm)	6σ TMU (nm)	Gate CD Tolerance (%)	Single Site TMU/T	Typical Sample Size	Wafer Average TMU/T
TEM	4.0	2.8	0	10.8	11.3	10	2.82	5	1.31
AFM	1.0	2.6	0	0	2.6	10	0.66	9	0.24
OCD	0	0.6	2.0	0	2.1	10	0.52	27	0.50
SEM	1.0	2.0	3.0	0	3.6	10	0.91	9	0.77

3.2.1. CD SEM sample-to-sample bias variation and OPC model verification

Sample-to-sample bias variation of CD SEM is understood and documented [4,11]. The known factors affecting bias in gate CD SEM measurements are line height, proximity to another line or shallow trench isolation (STI), sidewall profile and angle. Since the 130 nm technology node, CD AFM has been successfully used to study and characterize CD SEM bias variation for FEOL and BEOL applications.

Despite known bias variation CD SEM is still widely used for various engineering tasks and remains the main metrology used during OPC model creation and verification. CD AFM has so far been too slow and not sufficiently reliable to replace CD SEM. CD SEM has significantly better XY resolution (~ 4 nm) and is doing a much better job in imaging of complex 3D structures such as SRAM. CD AFM has a minimum space limitation and can't access spaces less than ~ 70 nm. Therefore, demand for an accurate and precise CD SEM is very high.

Over the last 2 technology nodes equipment manufacturers have achieved significant progress in improving CD SEM sample-to-sample bias variation. TMU (which includes bias variation) rather than precision (reproducibility) has become a selection and acceptance criterion for new CD SEM. Again CD AFM has been successfully used as a reference measurement system to asses TMU [12,13]. Figure 8 shows the variation of CD SEM bias through pitch observed for 90 nm technology poly-Si lines on 3 different SEM tools. The CD SEM bias for SEM_1 varies from 18 to 24 nm for pitch variation from 270 nm to 2000 nm. For the same pitch range SEM_2 and SEM_3 show less than half the bias variation at 3 nm. All systems have precision or reproducibility below 1 nm (3σ) and, therefore, in all 3 cases TMU is fully controlled by sample-to-sample bias variation. Figure 9 shows similar CD SEM bias variation data obtained for the 65 nm technology poly-Si gate. Once again SEM_2 and SEM_3 show similar CD bias through pitch variation of 3 nm. Figure 10 presents CD SEM bias through pitch variation for the 65 nm resist lines. SEM_2 and SEM_3 performed similarly and demonstrated CD bias through pitch variation of 4 nm.

Figure 11 shows an example of data collected for the 65 nm technology poly-Si gate OPC. The SEM_2 CD SEM was used for this data collection. Corresponding CD SEM bias variation for SEM_2 has been presented in Fig. 9. With AFM TMU estimated for this experiment at ~ 0.7 nm (3σ), and SEM precision at ~ 0.5 nm (3σ), the overall correlation between CD AFM and CD SEM data is excellent and CD SEM bias variation is likely does not exceed 2.5 nm (*cf.* Table 1).

3.2.2. OCD sample-to-sample bias variation and model verification

Modern OCD is capable of unprecedented line CD precision of 0.3 nm (3σ). OCD has become the main deep sub-micron CD metrology used for patterning process control. However, despite the wide recognition of OCD as the most precise CD metrology technique, two important questions often remain unanswered: (1) what is the TMU of OCD measurements and, (2) what is relation between CD's measured by OCD on special OCD structures and CD's of real IC's? We will try to answer the first question in this section and address the second question in section 3.3.

Once again as in the case of CD SEM, sample-to-sample bias variation can be a significant component of OCD TMU. One trivial and well know example of OCD sample-to-sample bias variation is line CD or height non-linearity. Figure 12 shows comparison of OCD and AFM data for photoresist line height. Since the Z-scale of the AFM has been verified with NIST traceable step standard, this data shows an OCD linearity problem. Non-linearity of the OCD data can be relatively easily detected during OCD model verification. In most cases, the OCD model can be fixed, or at least the data can be adjusted. Since the non-linearity is systematic, it can be excluded from OCD TMU. Unfortunately, the non-linearity is not the only source of OCD sample-to-sample bias variation. Figure 13 demonstrates a case where OCD bias varies with pitch. Once again CD AFM has been used as a reference tool to measure OCD bias variation. In this case CD bias variation is also systematic but it depends not only on line CD itself. Bias correction is still possible, but getting more complex and impractical. The systematic bias variation is usually caused by a non-perfect OCD model, and can therefore be fixed. However, to be fixed, it needs to be detected and properly characterized. Since CD SEM itself is not free from the sample-to-sample bias variation effects, CD AFM is virtually the only tool capable of this task.

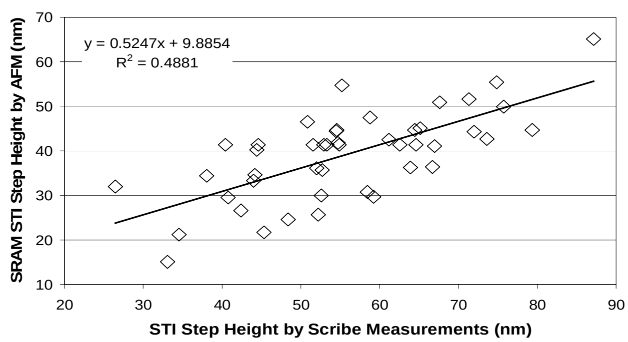

Figure 7. Correlation between post-CMP STI topography measured at scribe structure by profilometer and topography measured by AFM in the middle of SRAM array.

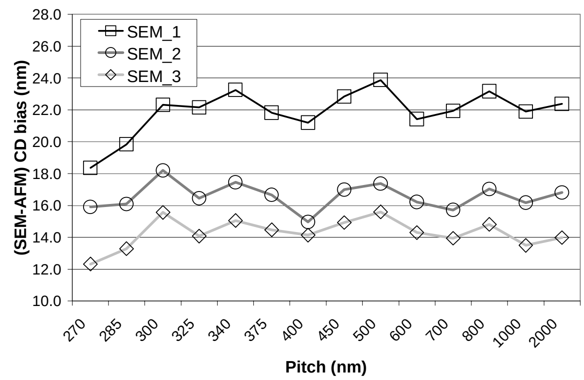

Figure 8. Through pitch variation of CD SEM bias observed for 90 nm technology node poly-Si lines on 3 different SEM tools.

Random OCD sample-to-sample bias variation is hard to measure and impossible to correct for. Some possible reasons for the random bias variation in OCD could be: (1) sample-to-sample variation of optical properties and film thicknesses of the stack not comprehended by the model (fixed parameters of the model), (2) change in line profile not captured by the model (deviation from assumed profile geometry), and (3) sample-to-sample variation in wafer alignment (not to be confused with dynamic repeatability). It is very difficult to separate this random component of OCD TMU from measurement uncertainty of the reference tool especially if these values are comparable [12, 13]. An attempt to make an estimate of OCD random sample-to-sample bias variation is shown in Table 1. This estimate is based on lot-to-lot variation of the difference between the lot average CD's measured by CD AFM and OCD, or by CD SEM and OCD. An example of such lot-to-lot comparison of the lot average CD by AFM and OCD is presented in Figure 14. It is an assumption that random sample-to-sample bias variation is a dominating contributor to the lot average measurement uncertainty since the repeatability component of the TMU should be minimized by averaging over a large number of independent but similar measurements. Random scale variation of the reference tool is also contributing to the lot average TMU and, therefore, should be removed from the OCD bias variation estimate [14].

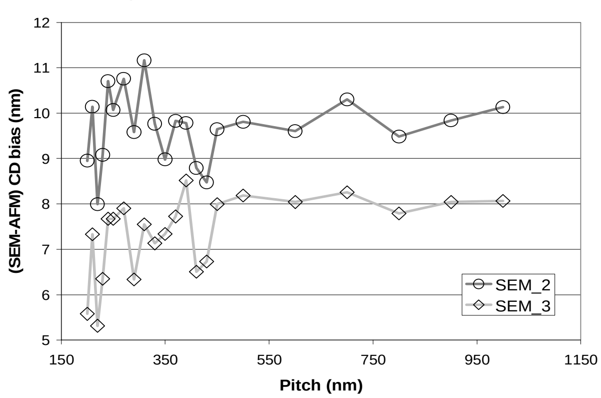

Figure 9. Through pitch variation of CD SEM bias observed for 65 nm technology node poly-Si lines on 2 SEM tools.

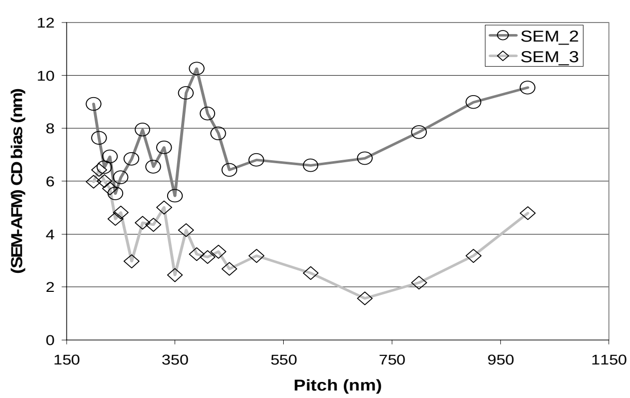

Figure 10. Through pitch variation of CD SEM bias observed for 65 nm technology node resist lines on 2 SEM tools.

3.2.3. Internal CD standard creation

In absence of NIST traceble line CD standards, AFM has been successfully used by semiconductor companies as a reference tool for internal absolute calibration of other CD metrology tools. Recently, similar methodology has been implemented by NIST to generate the first line CD standard [5]. In both cases high-resolution TEM (calibrated based on the Si atomic lattice spacing) is used for calibration of the reference CD AFM (Fig. 4). Once the CD AFM is calibrated, the “golden” sample is used to monitor the reference tool accuracy (Fig. 15). Since CD AFM bias is material and layout independent it can be used to calibrate line CD artifacts made of various materials with layout suitable for OCD or CD SEM calibration. CD AFM measurement does not damage the artifact and, therefore, long-term monitoring of the artifact CD is possible. The monitoring helps to detect CD drift caused by the electron beam (SEM) or UV-light (OCD) interaction with the artifact.

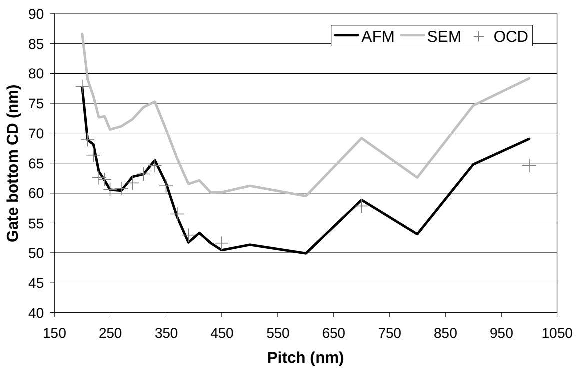

Figure 11. Through pitch variation of poly-Si lines CD measured by CD SEM, CD AFM and OCD.

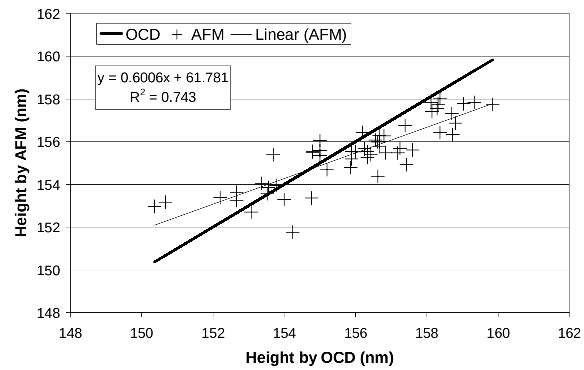

Figure 12. Correlation between OCD and AFM data for photoresist line height.

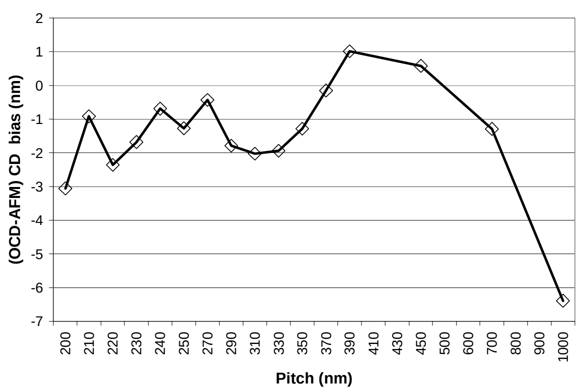

Figure 13. Through pitch variation of OCD bias observed for 65 nm technology node poly-Si lines.

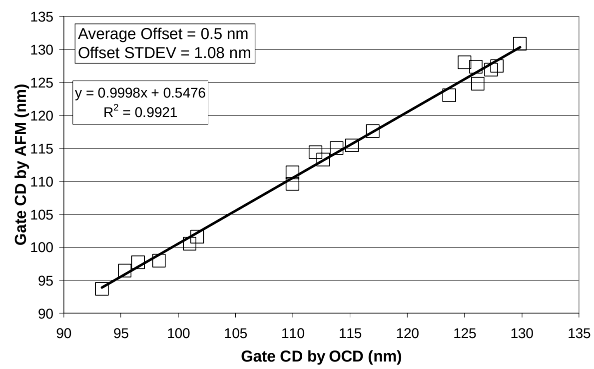

Figure 14. Correlation between the lot average poly-Si line CD measured by OCD and CD AFM for 130 nm technology node.

3.3. Across IC CD verification: OCD vs. real circuit CD

Today OCD is the main deep sub-micron CD metrology used for patterning process control. It has the best known precision and one of the best TMU (see Section 3.2). OCD is widely used for lot-to-lot, wafer-to-wafer, die-to-die and even across die CD control. The main disadvantage of OCD is use of special test structures for CD measurements. OCD can’t be performed on real IC. Therefore, before one can rely on OCD for IC CD control, the relationship between CD measured by OCD on special OCD structure and CD’s of real IC should be understood.

Why would lines drawn identically and having identical immediate proximity (pitch) be different? Let us review a few possible mechanisms of this phenomenon. Unfortunately, most of semiconductor processes (lithography, plasma etching, wet cleanup, etc.) have so-called macroloading effects. For example, the average density of poly-Si (gate) will affect plasma etching and cleanup poly-Si removal rates as well as CD’s of resist lines printed by lithography. The average poly-Si density is changing across the IC and this may cause CD offset between OCD and real IC.

Deep sub-micron lithography is extremely sensitive to wafer topography. Across IC CD variation depends strongly on post-CMP STI topography [15]. OCD structures are usually placed over large and flat area with an ideal topography. Real circuits are placed over STI layout and, therefore, their CD's will be affected by and vary with the STI topography.

Another source of discrepancy is potential OPC errors. OCD structures have a simple 1D layout. Real IC layouts are often complex and pose much higher risk of erroneous or non-ideal OPC. It is important to realize that CD offset caused by all three effects (macroloading, topography and OPC) may vary in time. The offset variation may be triggered by process or process tool changes. One example of OCD to IC CD offset variation is presented in Figure 16. The reported value is OCD to CD AFM offset observed on 130 nm technology node material. Every data point is an average of a large number of independent measurements (lot average). Estimated TMU of CD AFM for the reported measurements is less than 1 nm (3σ). The offset has been monitored for several weeks. The value of the offset and its variation during this experiment is significant with respect to the CD metrology budget of the 130 nm technology node.

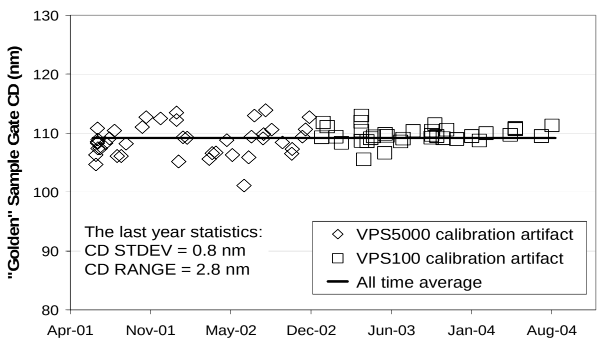

Figure 15. The long-term stability of CD AFM calibration.

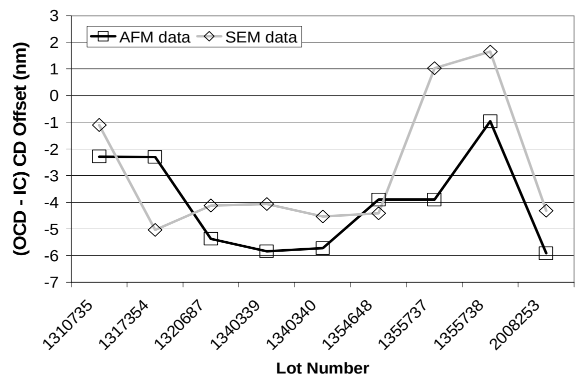

Figure 16. The variation of CD offset between the OCD structure line and the IC transistor gate.

3.4. Re-measuring the same structure through IC processing

Gate sidewall spacer (GSS) is an important element of modern CMOS integration. The deep sub-micron technologies have very strict (comparable to the gate CD) tolerances for the spacer thickness variation. Today thin film metrology is used to control thickness of sidewall spacers. However, accuracy and precision of this approach is no longer satisfactory. There is a strong demand for a new metrology which will measure thickness of sidewall spacer directly. OCD is a good candidate for this task. Once again, accuracy and TMU of OCD data need to be verified. Today TEM is widely used to verify and calibrate sidewall spacer OCD models. CD AFM can compete with TEM in TMU of GSS thickness measurements but also can quickly and non-destructively produce a large amount of valuable data. Figure 17 shows results of OCD model verification by using CD AFM as a reference tool. Discrepancy between OCD and AFM data is apparent. Further development of the OCD model is required.

Sidewall spacer formation is sensitive to various proximity (micro) and macroloading effects. Therefore, the GSS thickness needs to be monitored across IC and also for various transistor layouts. Moreover, process and integration engineers want to know evolution of the GSS through sequential steps of the gate processing. To get such information one would like to measure exactly the same gate several times through the processing. CD AFM is ideally suited for this type of work. It is important to note that sample-to-sample bias variation is minimal for CD AFM and, therefore, no bias correction is needed through the measurement. Figure 18 presents an example of such study. One gate with about 80 nm thick GSS went through the series of process steps including 2 RIE and 1 post-RIE cleanup. Only the first RIE has modified gate CD and profile significantly. The cleanup and the second RIE had only a minor effect on gate profile and CD.

3.5. Line edge and line width roughness measurements

CD AFM is a complementary to CD SEM line edge (LER) and line width (LWR) roughness metrology which offers some advantages. CD AFM can measure LER at any specified height of the gate. It is impossible to extract LER at specific height from the CD SEM data. CD SEM averages the line edge signal over the whole sidewall and, therefore, has a tendency to smooth and underestimate LER. Figure 19 demonstrates LWR data obtained on 90 nm technology material using CD AFM. As can be seen from the figure, gate CD measured at the middle of the gate does correlate with the bottom CD but the middle and bottom LWR's are not necessarily the same. For instance, structure A shows slightly better (-0.4 nm) middle LWR even as structure B shows the reverse trend (+0.6 nm). Our studies indicate that for this type of measurement, CD AFM is capable of 0.54 nm (3σ) LWR precision and, therefore, observed differences are at the limit of statistical significance. Reported precision for LWR measurements by CD SEM varies from 0.3 to 1.1 nm (3σ) [16]. Therefore, AFM precision of the LWR measurements is close to the top of CD SEM capability.

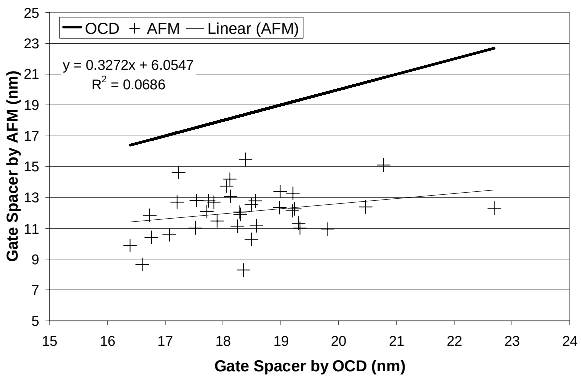

Figure 17. Correlation between the GSS thickness measured by OCD and CD AFM.

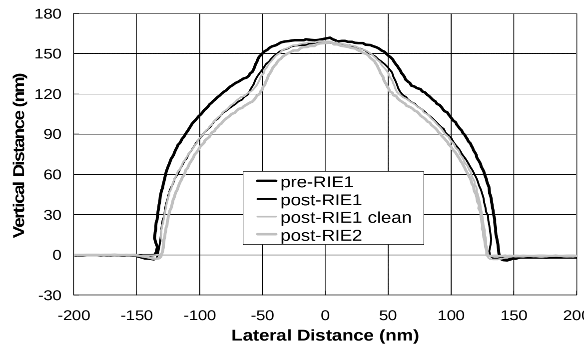

Figure 18. The GSS thickness and profile variation measured by CD AFM through IC processing.

XY spatial resolution of LWR and LER measurements may be considered as a disadvantage of CD AFM. The smallest flared probes can provide XY resolution of ~ 20 nm. This resolution can be achieved with the smallest rounded flared probes or regular rectangular flared probes but with scanning at 45° to the line axis. Data presented in Fig. 19 has been obtained with ~ 130 nm rectangular flared probe and the 45° scan. As recent CD SEM studies indicate [16], the lower spatial frequency components (less than 5×10^{-2} nm^{-1}) contribute to the poly-Si LWR the most. Therefore, the 20 nm XY resolution of CD AFM should be sufficient for accurate LWR and LER measurements.

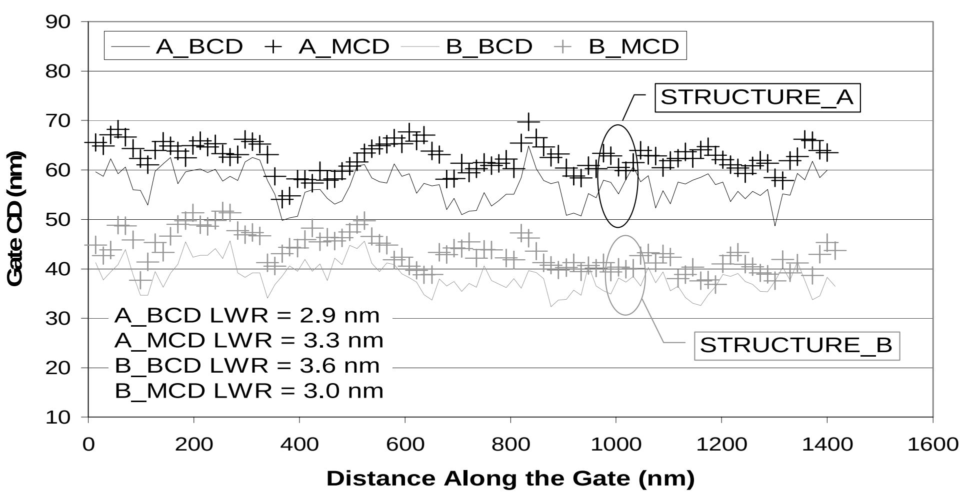

Figure 19. The LWR measured for poly-Si lines using CD AFM is shown. The data were collected with rectangular flared probe scanning at 45 to the poly-Si line axis. Both the bottom (BCD) and the middle (MCD) of the line LWR are presented.

3.6. Non-destructive 3D CD metrology

CD AFM has been used successfully for variety of engineering tasks in deep sub-micron semiconductor technology development. In this section we will present only two representative examples of such data. Figures 20 and

21 illustrate use of AFM for 3D characterization of interconnect via [17]. In the dual-damascene interconnect process [18] via anti-reflection coating fill is used to protect the bottom of the via during trench plasma etch (Fig. 21). Thickness of this via bottom fill is critical for the process. AFM can be effectively used to monitor variation of the via bottom fill thickness across wafer and IC (layout dependent thickness).

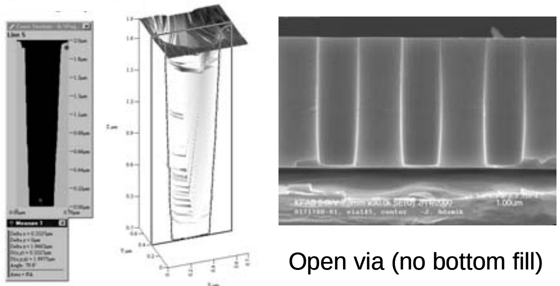

Figure 20. AFM and XSEM images of interconnect via.

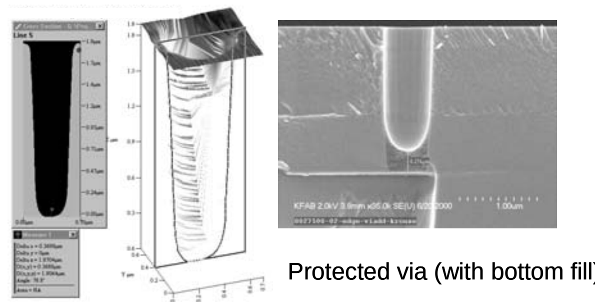

Figure 21. AFM and XSEM images of interconnect via filled with anti-reflection coating.

Another example of 3D CD metrology is presented in Figure 22. The figure shows 3D CD AFM image of the complex gate structure. Figure 22 can be used for simultaneous evaluation of line CD, height, sidewall angle and LWR.

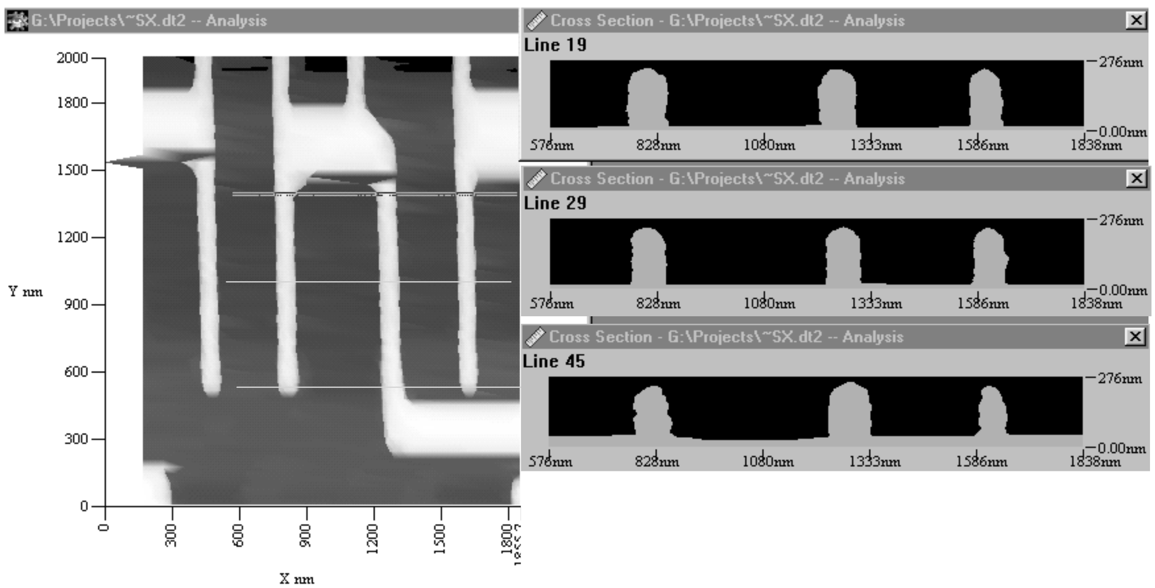

Figure 22. 3D CD AFM image (left) and 3 cross-sections (right) of the gate structure.

4. CURRENT LIMITATIONS OF AFM

According to the 1999 edition of ITRS AFM was expected to gradually replace CD SEM and OCD starting at ~ 50 nm technology node or about 2006-2008. Dramatic progress of OCD and the latest improvements in CD SEM apparently have discounted this projection. CD SEM and OCD are successful at the 65 nm node and likely to be key players at the 45 nm node and beyond. At the same time lack of attention from the semiconductor industry, limited resources and slowed down development of AFM CD metrology delays delivery of AFM tools to the industry. The situation is improving slowly, but even today very few equipment manufacturers are working on AFM metrology development.

Limitations of AFM have been analyzed elsewhere [1,6]. These limitations can be classified in several categories: probe size, probe geometry, probe wear or short lifetime, microscope throughput and reliability. The probe size limitations [1] are the most serious of all and demand immediate attention. Examining the probe size limitations one should consider separately the 1D and multi-dimensional applications of AFM. Smaller diameter cylindrical probes (Fig. 6) can be used for 1D AFM applications. Various manufacturing methods and materials are used to fabricate the cylindrical probes. Crystalline Si (c-Si) cylindrical probes are common. Carbon nanotube (CNT) cylindrical probes are commercially available but use of these probes is still very limited. The CNT probes are much more forgiving to AFM control errors and, therefore, have much longer lifetime. In reality "probe size" limitation is coming not from inability to fabricate cylindrical probe of the smaller diameter (current limit is ~ 15 nm) but rather from the failure to control position of such flexible probes near the surface. Probe flexibility and uncontrolled probe surface interaction (sticking or repulsion) obscure imaging and ruin AFM's accuracy and precision. However, if the only goal of 1D AFM metrology is to measure depth of trench or hole then one should be able to access and characterize spaces as small as ~ 30 nm. Once the goal is to characterize CD and profile of trench or hole, then the size limitation is stricter and 45-50 nm space is likely the limit of controllable AFM imaging with currently available cylindrical probes.

CD AFM metrology with cylindrical probes is limited to the cases of positive sidewall slope and fails if the sidewall is reentrant. Trenches and holes with reentrant sidewalls can be characterized with flared AFM probes only (Fig. 6). The smallest commercially available flared probe is ~ 50 nm in size and capable of ~ 70 nm trench or hole imaging. It is probable that the actual physical dimensions of these probes are smaller but the lateral dither required in CD AFM makes their "apparent" dimensions larger. CD AFM is likely capable of controlling even smaller flared tips (down to 10-15 nm probe shaft diameter). Therefore, in case of CD AFM the flared probe fabrication currently sets the limit.

CD AFM has limited XZ (sidewall profile) and XY (line edge roughness) resolutions. In both cases resolution is determined by the probe geometry. The XZ resolution is mostly limited by the radius of curvature of the flare. Typical XZ resolution for fresh c-Si probe is about 10 nm. This consists of the probe flare radius of curvature of ~ 5 nm, the "flying" distance between the probe and the surface of ~ 2 nm and the 3D adjustment of ~ 1 nm needed because of the YZ probe tilt (see section 2). Theoretically both XZ and XY resolutions can reach the required 1-2 nm through use of the XZ tilted and atomically sharp probes (Figure 23).

The XZ resolution degradation usually limits AFM probe lifetime. Therefore, even if the required 1-2 nm resolution is achieved it would be highly difficult to maintain it over the lifetime of the probe. This high resolution and reasonable probe lifetime can be reached only with true 3D non-contact and error free AFM. CD AFM developed in the early 90's by IBM was designed to operate in 2D non-contact mode. In reality, the probe regularly "touches" the surface because of AFM control deficiency or error. It is required for next generation AFM to resolve this problem. The probe flexibility and irregularity of the probe-surface interaction add complexity to the process. Special surface conditioning of the sample and the probe may be required to achieve CD AFM with nanometer resolution.

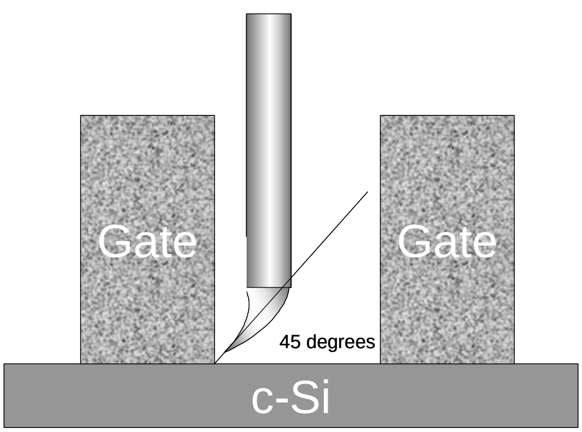

Figure 23. New probe design for high resolution AFM.

Another important limitation of modern AFM is its throughput. The throughput needs to be improved at least by a factor of 5 for AFM to be considered as in-line metrology suitable for SC manufacturing. Modern AFM spends about a minute per measurement while CD SEM and OCD spend ~ 15 sec and ~ 5 sec per measured site, respectively. The AFM measurement itself usually takes no more than 20-30 sec. Navigation to the site, descend to the surface and search for the feature of interest take the rest. This unfavorable ratio should be changed in the next generation of AFM through precise sub-micron probe positioning over the feature and efficient landing algorithms.

An idea of parallel multi-head AFM has been discussed numerous times. Many AFM operations could be performed in parallel: wafer pre-alignment, probe exchange and calibration, measurements on different dies or at least on the opposite sites of the wafer. Even a two-headed AFM should give the desired throughput and make AFM competitive with other CD metrologies.

The last, but possibly the most important limitation of modern AFM is its reliability. Today's AFM software is not reliable and too complex to be used in manufacturing environment. Dramatic progress has been made over the last few years in automated probe exchange and characterization. Still their robustness is not at the level required by the industry. To become competitive AFM should be as reliable and easy to use as electron and photon probe based tools.

5. THE FUTURE OF AFM

The semiconductor industry would benefit from wider use of CD AFM metrology. Today AFM is behind industry expectations, and AFM expansion is delayed. To change this situation AFM reliability should be improved to match the industry standards. The probe lifetime should reach a few days in manufacturing environment while maintaining high measurement resolution and precision. A thousand sites per probe would be a good lifetime to achieve. Therefore, further progress is needed in probe and scanning algorithm development. We are short in understanding of probe mechanics and physics of probe-surface interaction. New ideas are needed in AFM tool engineering.

The industry experts agree that deep sub-micron CD metrology requires synergy of complementary techniques such as OCD, CD SEM, CD AFM, TEM, XSEM, etc. Modern CD metrology has become very complex and demands a lot of engineering attention. For example, gate CD metrology usually consists of several operations (OCD, CD SEM and AFM). The data are used to control different components of gate CD variation (across lot, wafer, die, etc.). The data should be systematically checked for consistency between different metrology techniques. This complex and laborious process could be significantly simplified once CD AFM becomes a part of OCD or CD SEM tool. CD AFM could be used for instant SEM or OCD data verification and adjustment. Various feed forward schemes could be implemented. With intelligent AFM sampling plan, such a CD metrology system could maintain high throughput, operate with minimal engineering intervention and yet deliver data of unprecedented accuracy. The number of metrology operations, the data flow and the time needed to make a decision on lot disposition would be reduced.

6. ACKNOWLEDGMENTS

The authors would like to thank David Woodall, Henry Bradford, Luis Tristan, Jarvis Jacobs, Chad Kaneshige, and Jim Blatchford for help in data collection and stimulating discussions.

REFERENCES

[1] Bryan J. Rice et al, "CD Metrology for the 45 nm and 32 nm Nodes," Proceedings SPIE 5375, pp. 183-190, 2004.
[2] The transistor designers usually use the "gate length" term for the gate CD or for the poly-Si line width and the "gate width" term for the third gate dimension along the gate or along the poly-Si line.
[3] SEMI 1999. Document E89-0999 – Guide for Measurement System Capability Analysis.
[4] V. A. Ukraintsev, "Effect of bias variation on total uncertainty of CD measurements," Proceedings SPIE 5038, pp. 644-650, 2003.
[5] R. Dixon, A. Guerry, "Reference Metrology using a Next Generation CD-AFM," Proceedings SPIE 5375, pp. 633-646, 2004.
[6] H. M. Marchman, J. E. Griffith, "Scanned Probe Microscope Dimensional Metrology," *in Handbook of Silicon Semiconductor Metrology*, edited by A. C. Diebold, Marcel Dekker, Inc., New York, 2001, pp. 335-376.
[7] T. Trenkler, T. Kraiss, U. Maintz, P. Weidner, R. H. Pinto, „Improved Etch and CMP Process Control Using In-Line AFM," Proceedings SPIE 5375, pp. 486-493, 2004.
[8] P. A. Taylor, D. J. Dawson, "TIS, AFM, Interferometry, and Optical Profiler Correlation of Surface Roughness on Silicon Wafers," Proceedings SPIE 3619, pp. 128-133, 1999.
[9] The best lifetime and XY resolution has been achieved with carbon nanotube probes. Silicon probes provide comparable resolution but have shorter lifetime.
[10] Some progress on the nature of probe-to-sample interaction is definitely needed and long time expected. Our knowledge of physics and chemistry of probe-to-sample interaction is not adequate to the challenge CD AFM is facing.
[11] J. S. Villarrubia, A. E. Vladár, M. T. Postek, "A Simulation Study of Repeatability and Bias in the CD-SEM," Proceedings SPIE 5038, pp. 138-149, 2003.
[12] M. Sendelbach, C. Archie, "Scatterometry measurement precision and accuracy below 70 nm," Proceedings SPIE 5038, pp. 224-238, 2003.
[13] B. D. Bunday, M. Bishop, "Specifications and Methodologies for Benchmarking of Advanced CD-SEMs at the 90nm CMOS Technology Node and Beyond," Proceedings SPIE 5038, pp. 1038-1052, 2003.

[14] The Mandel regression analysis [12] has been used on the data presented in Fig. 14. Assuming TMU of the reference measurement system (CD AFM) of 2.0 nm (3σ) the TMU of the OCD equal to 1.45 nm (3σ) has been obtained. Using the OCD precision of 0.5 nm (3σ) bias variation of 1.36 nm (3σ) is calculated (*cf*. Table 1).
[15] The impact of STI step height on gate CD is mainly due to consumption of gate lithography focus margin.
[16] B. B. Bunday, M. Bishop, J. S. Villarrubia, A. E. Vladár, "CD-SEM Measurement of Line Edge Roughness Test Patterns for 193 nm Lithography," Proceedings SPIE 5038, pp.674-688, 2003.
[17] A. Ali, V. Ukraintsev, H. Sabri, M. Yang, "Nondestructive via in-hole profile characterization using atomic force microscopy metrology," JVST, B20(1), pp. 95-99, 2002.
[18] R. Havemann et al., "Dimensional Metrology Challenges for ULSI Interconnects," Proceedings of Characterization and Metrology for ULSI Technology, AIP conference proceedings Vol. 449, pp. 377-384, 1998.