

# Transition from precise to accurate critical dimension metrology

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## ABSTRACT

A new measurement system analysis (MSA) methodology has been developed at Texas Instruments (TI) to evaluate the status of the 65 nm technology critical dimension (CD) metrology and its readiness for production. Elements of the methodology were used in a previously reported scatterometry evaluation [1]. At every critical process level the precision, bias, linearity and total measurement uncertainty (TMU) were evaluated for metrology fleet over extended periods of time, and with the technology representative set of samples. The samples with variations that fully covered and often exceeded process space were pre-calibrated by CD atomic force microscope (AFM). CD AFM measurement precision was determined for every analyzed process level based on repeated measurements conducted over several days. The National Institute of Standards and Technologies (NIST) traceable standards were used to verify CD AFM line CD and scale calibrations. Therefore, for the first time the NIST traceability has been established for CD metrology at every critical process level for the entire technology. The data indicates an overall healthy status of the 65 nm CD metrology. Sub-nanometer accuracy has been established for gate CD metrology. The thorough CD metrology characterization and specifically absolute CD calibration were instrumental in seamless technology transfer from 200 nm to 300 nm fabs. The qualification of CD metrology also revealed several problems. Most of these are well-known from previous studies and should soon be addressed. CD scanning electron microscopy (SEM) has a systematic problem with bias of CD measurements. The problem is common for several front-end and back-end of line process levels. For most process levels, TMU of CD SEM is noticeably affected by sample modification inflicted by electron irradiation (shrinkage, charging, buildups, etc.). This causes problems, especially in the case of fleet TMU evaluation. An improved data collection methodology should be devised to minimize the impact of sample modification on fleet TMU measurements. The reported progress in semiconductor industrial CD metrology became possible after a recent breakthrough in line CD standard technology [2,3], recognition of CD AFM as an instrument for CD traceability [4,5] and development of the concept and mathematical tools for TMU analysis [6,7].

**Keywords:** Accuracy, critical dimension, bias variation, fleet precision, TMU, AFM.

## 1. INTRODUCTION

Establishing an accurate CD metrology is costly, but necessary for the success and competitiveness of a semiconductor technology [1, 7]. What are the key benefits of absolute CD measurements of integrated circuits (IC)? Reaching target performance of metal-oxide-semiconductor field effect transistor (MOSFET) is at the core of every semiconductor technology development. Various electrical performance and process simulation tools are used to design and predict characteristics of the new transistor. MOSFET gate CD and the sidewall profile are the main physical characteristics dictating transistor performance. An accuracy of gate CD metrology inputs is essential for predictability of physics based modeling and, therefore, for reducing the number of learning cycles needed for the targeted MOSFET performance. Simulation tools play a critical role in today's costly and highly competitive technology development.

Modern technology development is unthinkable without photolithography modeling and resolution enhancement technology. Knowledge of absolute CDs of printed patterns is critical for developing physics based photolithography simulators and optical proximity correction (OPC) models. Accuracy of the models depends on accurate CD metrology inputs. Proper RET choices and correct OPC models form the technology base. They are very expensive to correct and essential for technology success.

Sample-to-sample bias variation is often a dominate component of CD TMU in semiconductor technologies beyond the 130 nm node [1]. Uncontrolled process variation is the most dangerous source of bias variation and TMU. Just as feature dimensions shrink with each technology node, CD metrology techniques are operating at sensitivity limits, often with a marginal signal-to-noise ratio. In most cases, these uncontrolled process variations (and not the tool itself) set the level of "noise" and the technique's sensitivity limit. Even minor process variations may cause a noticeable CD bias shift through cross-correlation of optical scatterometry (OS) model parameters or SEM. For example, modification of a cleanup process may cause surface roughness or dopant concentration surface depletion and lead to changes in the poly

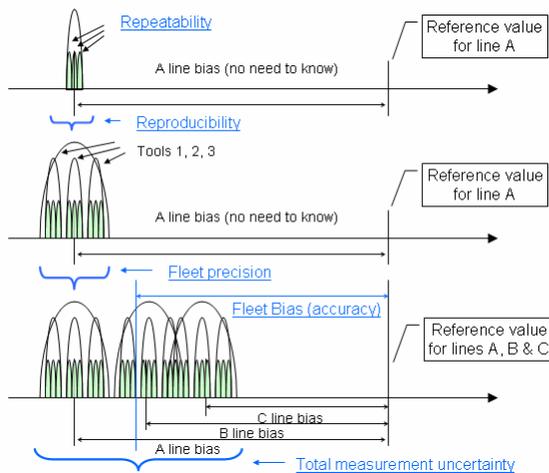
silicon optical and secondary electron appearance. Therefore, the knowledge of absolute reference CDs of test samples is needed to calibrate OS and SEM models, and to evaluate the impact of uncontrolled factors on TMU of CD metrology accuracy.

Accurate CD metrology is also useful in matching CD metrology techniques within a single fab, or between different fabs. It's a common practice to transfer technology from a single development fab to multiple manufacturing fabs. The technology transfer can be simplified with accurate CD metrology for all critical processes. Matching tools of the same type and supplier with a few internal CD standards should be relatively easy. In some cases the standards can't be shared between different tool types. In other cases, a limited set of standards does not represent the technology's process space. Therefore, a universal MSA methodology is needed to assess the accuracy of various CD metrology techniques operating at different process levels in different fabs.

This article covers a new MSA methodology developed recently at TI for the 65 nm technology node CD metrology qualification. The methodology is designed to establish an accurate CD metrology of the critical processes in semiconductor IC manufacturing, and its traceability to NIST units and standards. This work is based on a recent breakthrough in line CD standard technology [2,3], recognition of CD AFM as an instrument for CD traceability [4,5] and development of the concept and mathematical tools for TMU analysis [6,7].

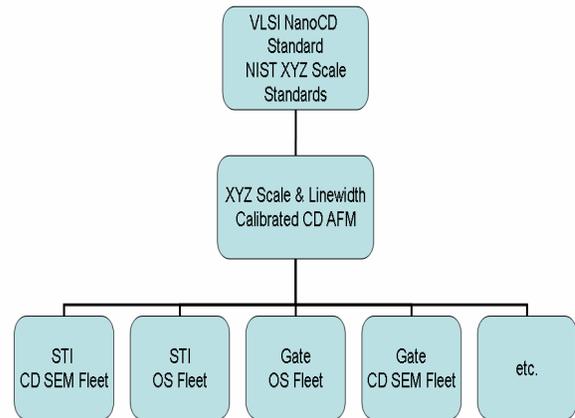
## 2. METHODOLOGY

Elements of the MSA methodology were used in the evaluation of OS readiness for 65 nm technology development and production [1]. This time complete MSA was implemented for 65 nm OS and SEM CD metrology qualification and release for production. The qualification included an assessment of precision, TMU, and bias (or systematic error) for the fleet of baseline metrology tools used for several critical technology processes. Complex relations between precision, TMU and bias for a single tool, and fleet of metrology tools, have been described before [1] and are illustrated in Figure 1.



**Figure 1.** Relations of time, tool and sample dependent components of metrology fleet TMU and bias.

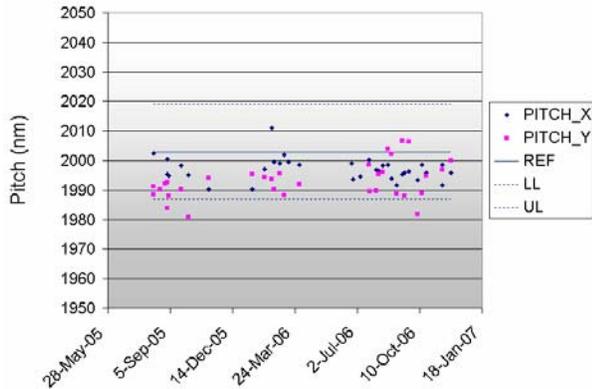
As follows from the figure, measurement bias is a function of time (reproducibility or precision), tool (tool-to-tool matching or fleet precision) and sample (material, line height, sidewall angle and profile, proximity to another line or object, etc.). Fleet TMU is defined by total bias variation with measurement-to-measurement, tool-to-tool, and sample-to-sample components. Fleet bias or accuracy is defined as an average systematic error of the fleet (bias between reported fleet average and reference value). Since fleet bias is sample dependent, an accuracy of fleet cannot be evaluated using external pre-calibrated standards. A representative set of standards must be fabricated using a specific technology in a specific fab on a specific manufacturing tool. The set of samples should cover the technology multi-dimensional process space as fully as possible (lithography focus-exposure conditions, material composition, sidewall profile, equipment, etc.). The samples are then calibrated with CD AFM pre-calibrated using the NIST traceable XYZ-scale and line CD standards. This calibration technique is similar to the NIST line CD standard calibration procedure [2, 4]. Figure 2 illustrates the MSA process flow. The internal standards were measured several times until there was a high level of confidence in the CD AFM data, and the uncertainty of the data (reproducibility) was well defined and did not



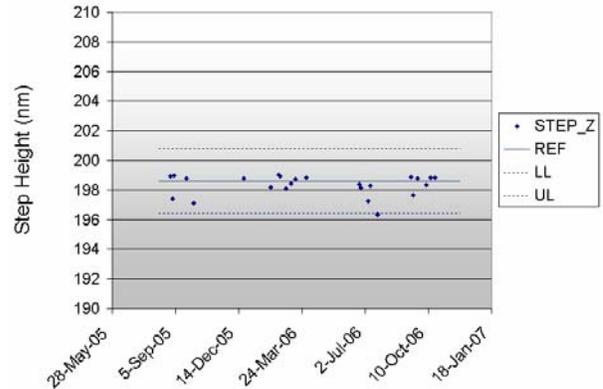
**Figure 2.** The uncertified NIST traceability of 65 nm CD metrology and process flow of the MSA.

change significantly with additional rounds of data collection. More than one AFM probe was used on each sample to make sure that probe-to-probe data variation was insignificant. The frequency of AFM probe calibration was modified for different rounds of data collection to minimize potential AFM systematic errors related to probe wear [1].

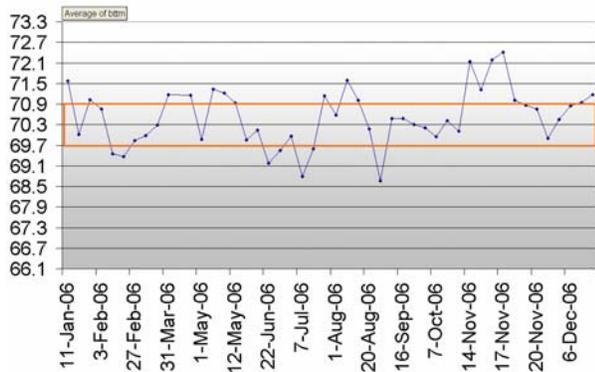
CD AFM scale and probe width calibrations were verified systematically during the internal standards calibration conducted January to March of 2006 (Figures 3-5). As seen in the figures, the XYZ scale calibration was within a 0.95 confidence level (CL) uncertainty of the correspondent VLSI standard. In general, overall line CD calibration remained within a 0.95 CL uncertainty of  $\pm 0.6$  nm of the VLSI NanoCD standard, with the full range of line CD uncertainty of 2.2 nm. Since reference CDs of the internal standards are averages of data collected over several days, the reported (Fig. 5) uncertainty of CD AFM probe calibration does not represent the uncertainty of the reference data. The later will be calculated for every set of internal standards designated for the specific process.



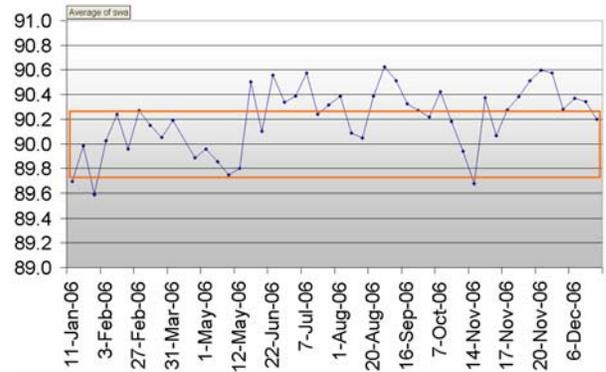
**Figure 3.** Stability of the reference CD AFM lateral (X & Y) scale calibration. The dotted lines show the upper and lower uncertainty limits of the VLSI pitch standard for CL of 0.95.



**Figure 4.** Stability of the reference CD AFM vertical (Z) scale calibration. The dotted lines show the upper and lower uncertainty limits of the VLSI pitch standard for CL of 0.95



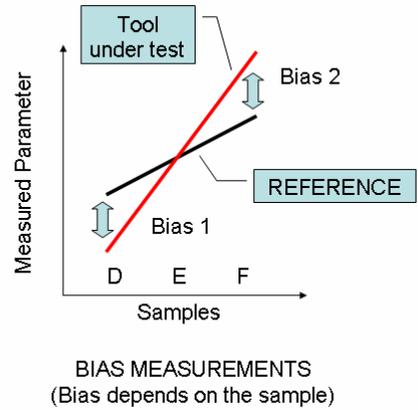
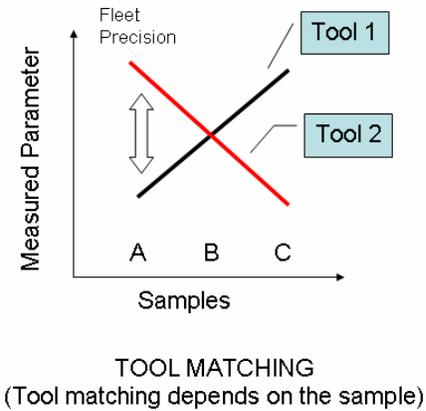
**Figure 5.** Stability of the reference CD AFM line CD calibration. The box shows uncertainty limits of the VLSI NanoCD line CD standard for CL of 0.95.



**Figure 6.** Stability of the reference CD AFM line sidewall angle calibration. The box shows *estimated* uncertainty limits of the VLSI NanoCD line CD standard for CL of 0.95 [10].

The ultimate goal of the MSA is to estimate an uncertainty of measurement on an arbitrary baseline sample on an arbitrary baseline metrology tool. As depicted in Figure 1 the uncertainty could be split in two components: the TMU (or “random” fleet error [8]), and the fleet average bias (or fleet systematic error). Single tool and even fleet precisions (or reproducibilities) are the secondary unknowns needed to identify contributions of different sources of the uncertainty, and to focus improvement work on the main component. As previously noted, measurement bias is time, tool and sample dependent. Therefore, the selection of test samples (standards) used to estimate tool-to-tool matching (fleet precision), as well as the selection of tools and samples to estimate fleet bias (fleet accuracy), are important. Figures 7 and 8 illustrate the importance of test sample selection for fleet precision, TMU and average bias measurements. The match is perfect if tool-to-tool matching is estimated using only the “B” sample (Fig. 7). The tool-to-tool matching worsens for samples “A” and “C”. Once measurement deltas for the two tools and all samples are averaged, the match is (misleadingly) perfect again. Similarly, if bias is measured using only the “E” sample, no bias

would be detected (Fig. 8). Measurements for samples “E” and “F” show biases in opposite directions. Once again, averaging biases for all samples would result in zero average bias (or systematic error). The TMU will be determined by the biases observed for various samples including non-zero biases for the samples “D” and “F”.



**Figure 7.** An illustration of impact of spectrum of test samples on tool matching and fleet precision measurements.

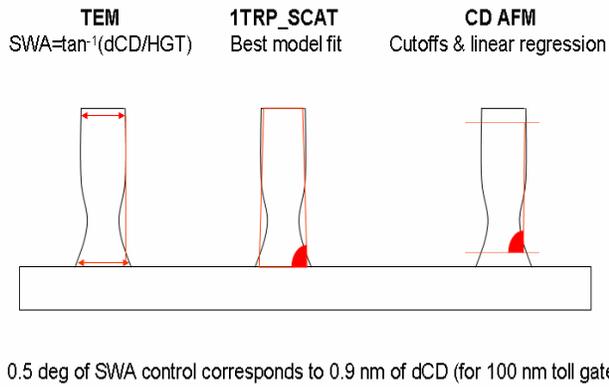
**Figure 8.** An illustration of impact of spectrum of test samples on fleet bias measurements.

Therefore, to reflect the complex dependence of measurement bias (error) on time, tool and sample, a statistically significant number of test samples (internal standards) were used in the MSA to represent the entire process space as fully and uniformly as possible [9]. Every test sample (pre-calibrated measurement site) was measured multiple times over extended periods of time (more than 5 days) on every baseline metrology tool. To calculate precision (single tool or fleet) variances of all measurements were calculated for each individual sample (site). The average variance and the standard deviation of the average were computed assuming normal distribution of measured values. Every measurement was referenced to the corresponding reference CD and used to calculate fleet TMU, correlation, slope (or linearity) and average fleet bias (or systematic error). The same procedure was used for every evaluated process level.

Figure 6 shows the CD AFM measurements of sidewall angle (SWA) for the VLSI NanoCD poly silicon line standard. According to the manufacturer, the standard uncertainty of line CD at any height is  $\pm 0.6$  nm, with confidence of 0.95. The standard’s SWA uncertainty is not certified. Nevertheless, our estimate for 100 nm toll poly silicon line shows it should be about  $\pm 0.26$  degree if the top and the bottom CDs are within the standard specification [10]. As seen in Figure 6, the SWA measured by CD AFM was within the expected range at the time of the MSA, but shifted up about 0.35 degree in June 2006. The shift was caused by an intentional change in CD AFM scanning parameters recommended by the AFM supplier to increase the probe’s lifetime.

Getting expected SWA values for vertical well-defined NanoCD poly silicon line does not necessarily mean that CD AFM can be used as a reference tool for verification of accuracy of SWA measurements by OS or any other technique. As previously noted [1], CD AFM is virtually “blind” for the bottom 10-15 nm of line sidewall. Also, definitions of SWA used by CD AFM, OS and transmission electron microscopy (TEM) differ significantly (see Figure 9). CD AFM still can be used for verification of line CD at any given height that can be calculated with OS or other sidewall sensitive technique data. Such calibrations should be done with detailed attention to what the CD AFM is measuring and how these measurements are affected by CD AFM sidewall resolution [1]. Despite the problem direct comparisons of SWA data will be reported in this article. The reader should remember that CD AFM SWA data is not NIST traceable.

Another CD metrology challenge faced by the industry is verification of accuracy of hole (contact and via) diameter measurements. Figure 10 illustrates potential problems with CD AFM hole diameter measurements. In cases A and B, AFM probe doesn’t reach the bottom of the hole. The depth and the bottom diameter will be measured incorrectly. Hole diameter measurements in cases C and D will be affected by the limited sidewall resolution of CD AFM. Impact of these factors on CD AFM hole diameter measurement is difficult to predict and will depend on sidewall roughness and specific AFM probe dimensions and geometry. TEM of holes should be used in parallel with CD AFM to make sure reference data are not obscured by problems presented in Figure 10 or any other unexpected complication. CD AFM hole diameter data is not NIST traceable and will be treated in the MSA as such.



**Figure 9.** Differences in SWA definition by TEM, OS and CD AFM.

Therefore, the following assumptions were used during the MSA:

- Calibrated CD AFM has sample independent zero bias of line CD measurements,
- Time, tool and sample dependent uncertainties of CD measurements for all analyzed metrologies can be adequately described using the normal distribution statistics,
- Samples generated for this study properly represent multi-dimensional space of every analyzed baseline process.

### 3. RESULTS

The following eight CD metrologies were identified as critical for technology control and representative for an evaluation of overall metrology status of the 65 nm technology:

- Shallow trench isolation (STI) post plasma etching OS,
- STI post plasma etching CD SEM,
- Gate post plasma etching OS,
- Gate post plasma etching CD SEM,
- Gate the low dose dopant (LDD) sidewall spacer OS,
- Gate the high dose dopant (HDD) sidewall spacer CD SEM,
- Contact post plasma etching patterning CD SEM,
- Interconnect trench post plasma etching patterning CD SEM.

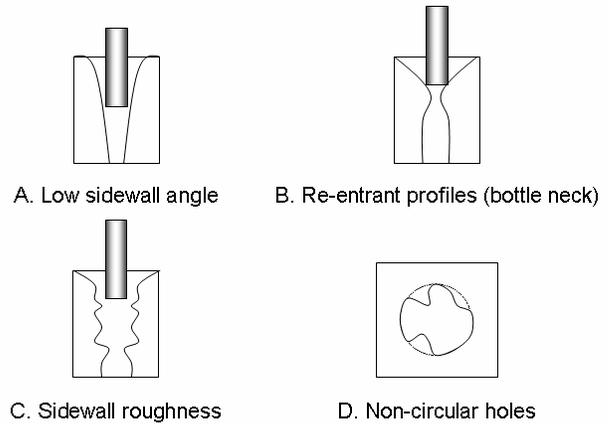
For every application, a set of wafers representative for the specific process was created. To cover the process space, so-called focus exposure matrix (FEM) wafers were used. The scanner's focus and exposure change systematically across the FEM wafer and every scanner's shot (die) represents a unique point in the process space. To enhance statistics and to test across wafer effects, wafers with the optimal but constant focus and exposure (FE) were also used in the study.

For most applications, the precision of the single CD AFM measurement for lateral and vertical CDs is about 1.5 nm ( $3\sigma$ ). The uncertainty of the reference CDs was improved by averaging data from multiple rounds of the AFM measurements. Uncertainty of CD AFM data for every specific application will be reported.

The pre-calibrated wafers were then measured on every baseline metrology tool over an extended period of time (more than five days). The data collected on all tools over the test period were pooled together. The following values were calculated for every application:

- Fleet bias averaged for all sites, tools and measurement events;
- Fleet linearity calculated for all sites, tools and measurement events [11];
- Correlation between fleet under evaluation and reference data [12];
- A single tool precision statistically averaged (using variances) for all sites and tools;
- Fleet precision statistically averaged (using variances) for all sites;
- Fleet TMU calculated using data collected for all sites, tools and measurement events.

Mandel's regression was used to estimate fleet TMU [7,13]. Every measurement (site, tool, repeat) was treated as an independent event and correlated to the corresponding site specific reference value. The same reference value was used multiple times for measurements on various tools and at different times. Fleet TMU calculated with this approach

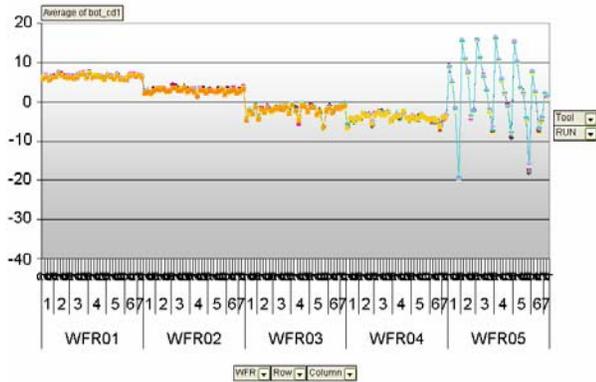


**Figure 10.** Potential problems with hole diameter measurements by CD AFM.

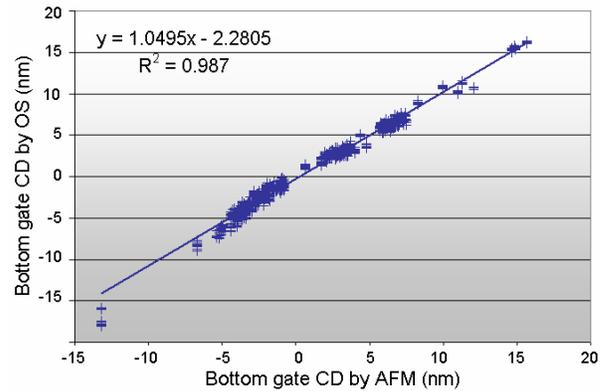
included sample-to-sample, tool-to-tool and measurement-to-measurement components. Uncertainty of the bias measurement related to the uncertainty of the reference CD AFM data was excluded from the fleet TMU through the use of Mandel's analysis.

### 3.1. Gate CD metrology

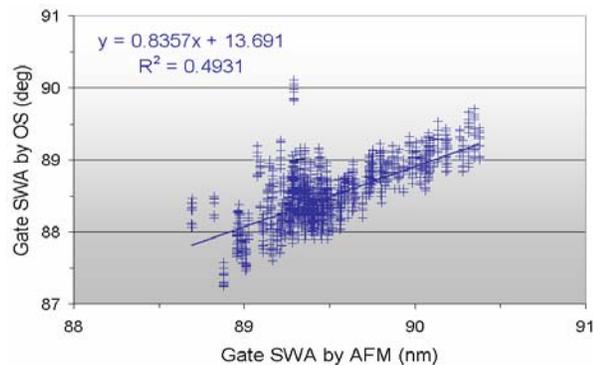
As technology computer aided design (TCAD) simulations suggest gate post etching CD metrology is the most critical metrology for transistor electrical performance control. Two metrologies are used at this process level. OS is used for transistor CD targeting and process control. CD SEM is used to monitor biases between CDs of the OS targets and real transistors within controlled ICs. Three parameters used to characterize the gate are: height, bottom CD and SWA [1]. Figure 11 shows gate CDs by site as measured by OS on one FEM and four constant FE wafers used in the gate MSA. Figure 12 presents the correlation between OS and reference data for the gate bottom CD of 260 nm pitch structure. The total number of pre-calibrated sites is 170. The total number of OS measurements for 3 baseline tools and 7 repeats is 3570.



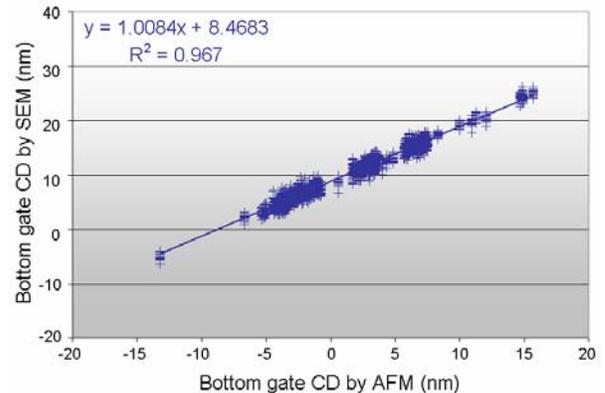
**Figure 11.** The bottom gate CDs by site as measured by OS fleet.



**Figure 12.** The correlation between OS and reference data for the gate bottom CD of 260 nm pitch structure.



**Figure 13.** The correlation between OS and reference data for gate SWA of 260 nm pitch structure.



**Figure 14.** The correlation between gate CD by SEM and the bottom gate CD reference data.

The data showed an excellent correlation of 0.99 and a slope of 1.05. The fleet bias was a minor -0.2 nm. The fleet TMU calculated with reference data uncertainty of 0.85 nm ( $3\sigma$ ) was 0.82 nm ( $3\sigma$ ). The TMU slightly exceeded the fleet precision of 0.68 nm ( $3\sigma$ ). An average single tool precision was 0.47 nm ( $3\sigma$ ). It appeared that OS sample-to-sample and tool-to-tool bias variations were minor and single tool reproducibility was a dominating contributor to the TMU. Overall results are satisfactory. The OS can control processes with bottom CD tolerance of  $\pm 4$  nm ( $3\sigma$ ) assuming that TMU to process tolerance ratio (TMU/T) of 0.2 is acceptable.

Figure 13 shows the correlation between OS and reference data for SWA of the 260 nm pitch structure. As expected based on previously reported data [1], OS experienced some difficulty with gate SWA measurements. The correlation between OS and reference data was 0.70 with a slope of 0.84. The fleet bias was -1.0 deg, which may be attributed to

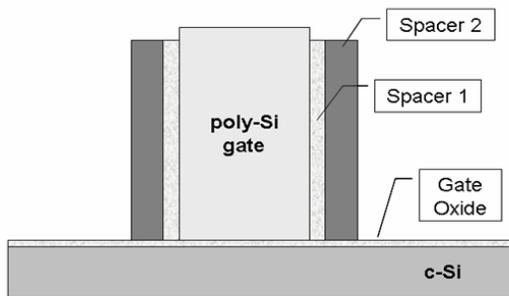
differences between SWA definitions of CD AFM and OS. The fleet TMU calculated with reference data uncertainty of 0.22 deg ( $3\sigma$ ) was 0.78 deg ( $3\sigma$ ). The fleet and single tool precisions were 0.47 deg ( $3\sigma$ ) and 0.19 deg ( $3\sigma$ ), respectively. Even assuming that most of the TMU comes from discrepancy between CD AFM and OS SWA definitions, one must admit that the OS fleet precision is high and at best the OS can support SWA process tolerance of  $\pm 1.6$  deg ( $3\sigma$ ) with TMU/T of 0.3. Therefore, based on available CD AFM reference data (untraceable to the NIST), the OS SWA precision and accuracy are marginal. Improvement of the OS metrology for gate SWA is needed.

Figure 14 demonstrates the correlation of gate CD by SEM and bottom CD reference data. The same five gate post etching wafers (Fig. 11) were used for CD SEM fleet evaluation. The data was collected on three CD SEM tools over five days. The correlation with reference data and the linearity are a good 0.98 and 1.01, respectively. The bias is 8.8 nm. The CD SEM gate fleet TMU calculated with reference data uncertainty of 0.85 nm ( $3\sigma$ ) was 2.31 nm ( $3\sigma$ ). The fleet and single tool precisions were 2.26 nm ( $3\sigma$ ) and 1.59 nm ( $3\sigma$ ), respectively. The data indicates that sample-to-sample bias variation does not contribute much to the TMU. The tool-to-tool matching and single tool reproducibility contributions are significant. The reproducibility (precision) of CD SEM measurements could be affected by selection of a non-unique target (arbitrary line of OS target has been used for the measurements). Nevertheless, our estimations show that contribution of line width roughness to the reproducibility of CD SEM measurements should not exceed 0.54 nm ( $3\sigma$ ). It was found, therefore, that CD SEM gate CD precision and tool matching are outside of the fleet specification. Work is in progress to improve CD SEM fleet performance for the gate CD measurements.

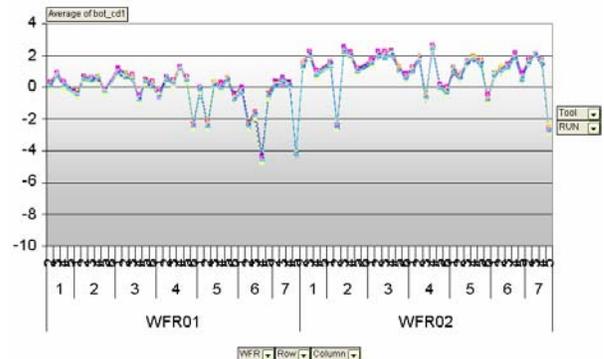
### 3.2. Gate LDD sidewall spacer CD metrology

Based on TCAD simulations of 65 nm technology MOSFET sensitivity, the gate LDD sidewall spacer metrology is the second most important CD metrology for the transistor performance control. OS is used to control the total gate bottom CD and the spacer thickness at this process level. The gate LDD sidewall spacer stack and OS model are illustrated in Figure 15. The OS model is similar to the gate model, but has an extra parameter - the sidewall spacer thickness [1]. To verify accuracy of the gate LDD spacer metrology the total gate bottom CD was calibrated by CD AFM at the post spacer etching process level. Two wafers with 68 pre-calibrated sites (260 nm pitch structure) were used for the MSA. The wafers were measured more than seven days on three baseline OS tools. Figure 16 shows the bottom gate CDs by site as measured by OS. Figure 17 presents the correlation between the OS and reference data. The data shows a correlation of 0.93 and a slope of 0.80. The fleet bias for the bottom gate CD at this level was -2.8 nm. The fleet TMU was estimated as 0.70 nm ( $3\sigma$ ) using uncertainty of the reference bottom gate CDs of 0.95 nm ( $3\sigma$ ). The OS single tool and fleet precisions for the bottom gate CD were 0.32 nm ( $3\sigma$ ) and 0.41 nm ( $3\sigma$ ), respectively. Corresponding OS single tool and fleet precisions for the thickness of LDD spacer were 0.17 nm ( $3\sigma$ ) and 0.21 nm ( $3\sigma$ ), respectively.

The OS provides a satisfactory fleet TMU (TMU/T is below 0.2) and acceptable accuracy for the bottom gate CD control at gate LDD spacer etching. The OS fleet precision is marginal, but acceptable for LDD spacer thickness control. An accuracy of OS measurements of LDD spacer thickness was not evaluated directly during the MSA. Based on previous [1] and current MSA results, a sufficient level of trust in the accuracy of the spacer thickness measurements is established.



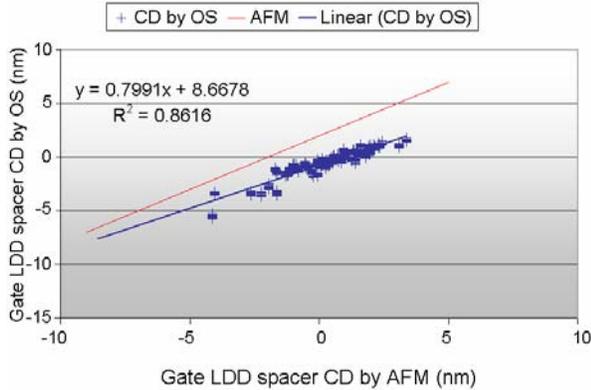
**Figure 15.** Gate sidewall spacer post etching stack and geometry.



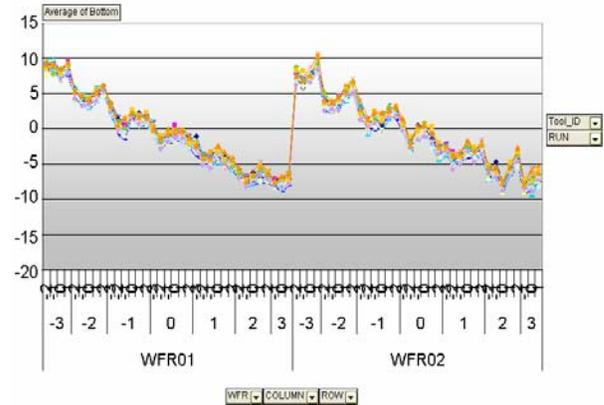
**Figure 16.** The total bottom gate CDs as measured by OS fleet at gate LDD spacer etching.

### 3.3. Gate HDD sidewall spacer CD metrology

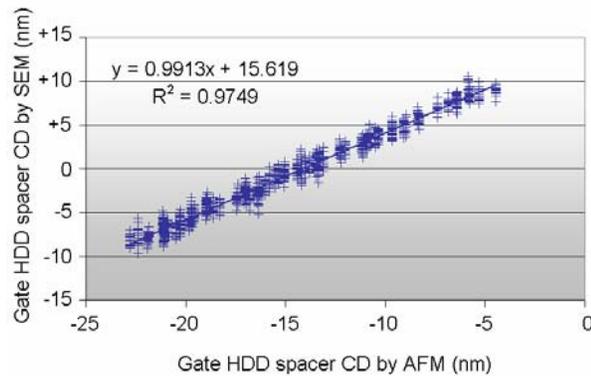
The gate HDD sidewall spacer dimensions define position of the MOSFET's source and drain with respect to its channel. The gate HDD spacer metrology was found critical for MOSFET targeting and control. The gate HDD sidewall spacer stack and geometry is too complex for OS modeling. Therefore, SEM is used to control the total gate bottom CD and spacer thickness at the HDD spacer etching process level. Two exposure matrix (EM) wafers with 70 pre-calibrated sites (260 nm pitch OS structure) were used for the MSA. The wafers were measured more than seven days on three baseline SEM tools. Figure 18 shows the total bottom gate CDs by site as measured by SEM. Figure 19 presents the correlation between the SEM and reference data. The data shows a correlation of 0.99 and a slope of 0.99. The fleet bias for the bottom gate CD at the HDD spacer etching was 14.2 nm (cf. to SEM bias of 8.8 nm at the gate etching). The fleet TMU was estimated as 2.1 nm ( $3\sigma$ ) using uncertainty of reference data of 1.1 nm ( $3\sigma$ ). The OS single tool and fleet precisions for the bottom gate CD were 1.3 nm ( $3\sigma$ ) and 2.0 nm ( $3\sigma$ ), respectively. The SEM fleet TMU/T ratio for the HDD sidewall spacer control was at an acceptable level below 0.2.



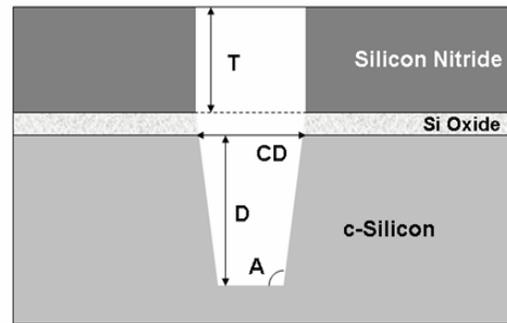
**Figure 17.** The correlation between the OS and reference data for the total bottom gate CD at gate LDD spacer etching.



**Figure 18.** The total bottom gate CD as measured by SEM at gate HDD spacer etching.



**Figure 19.** The correlation between CD SEM and reference data for the total bottom gate CD at gate HDD spacer etching.



**Figure 20.** STI post etching stack and geometry of the trench.

### 3.4. STI CD metrology

STI line CD defines the width of the MOSFET and directly impacts transistor performance. STI trench CD and sidewall profile are critical for transistor reliability and leakage control, as well as for the quality of STI fill and overall density of STI defects. Therefore, STI CD metrology is an important part of semiconductor technology. STI post etching stack and geometry of the trench are depicted in Figure 20. Four parameters are usually used to characterize the structure: silicon nitride thickness (T), depth (D), sidewall angle (A) and the top CD of the Si trench. The MSA is focused on the evaluation of TMU and the accuracy of the top trench and line CD measurements. Both OS and SEM analyses used 190 nm pitch OS structure with the line of 80 nm and space of 110 nm. Figure 21 shows site-by-site CDs of STI line as measured by OS fleet of three tools more than seven days on two FEM and three constant FE wafers. The

correlation between the OS and reference data is presented in Figure 22. The OS shows reasonable correlation of 0.93 and a slope of 1.16. The fleet bias is -0.8 nm. Using Mandel's regression and reference data uncertainty of 2.5 nm ( $3\sigma$ ), fleet TMU of OS is estimated to be 5.72 nm ( $3\sigma$ ). The uncertainty of STI CD reference data is impacted by the CD AFM probe-to-probe variation. Variation of probe's apex radius of curvature (or so-called probe's vertical edge height [5]) changes the exact height at which STI CD is measured. Since STI sidewall is sloped, the height change noticeably affects STI line CD measurement. For tested STI OS CD metrology, sample-to-sample bias variation is significant. It is difficult for the OS to follow true STI CD variation. The fleet TMU noticeably exceeds the fleet precision of 1.2 nm ( $3\sigma$ ) and single tool precision of 0.5 nm ( $3\sigma$ ). The problem was detected during OS evaluation [1] and caused by the cross-correlation between the OS model's parameters, such as line CD, STI depth and silicon nitride thickness. It seems that the current generation of OS tools has reached its limit. The TMU of STI line CD OS measurement is unacceptably high.

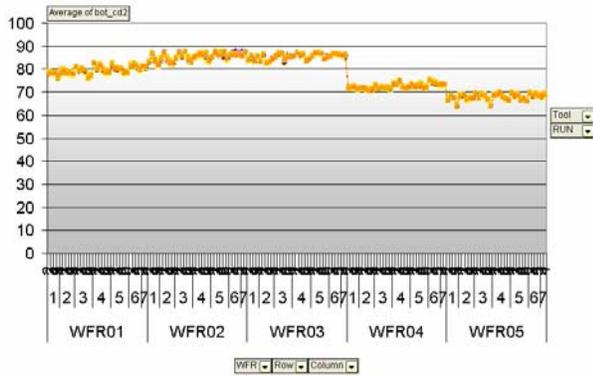


Figure 21. STI line CD as measured by OS fleet.

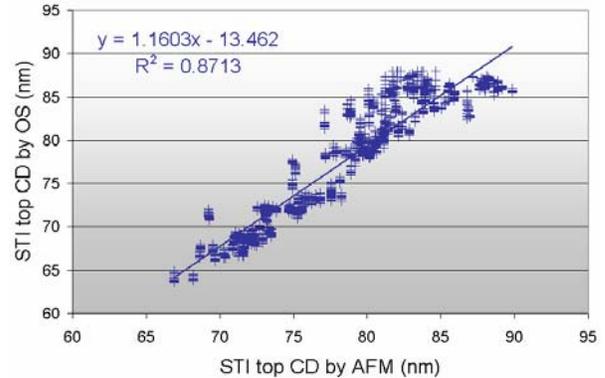


Figure 22. The correlation between OS and reference data for STI line CD.

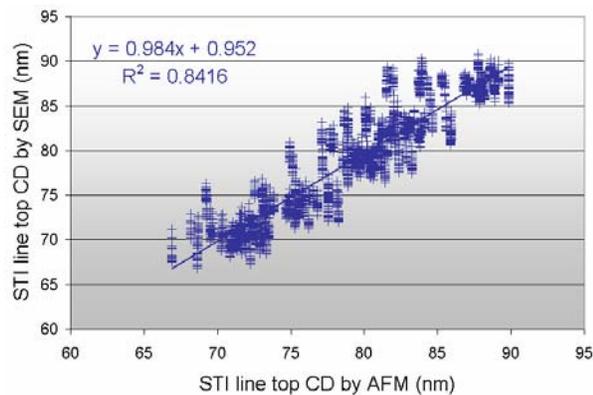


Figure 23. The correlation between CD SEM and reference data for STI line CD.

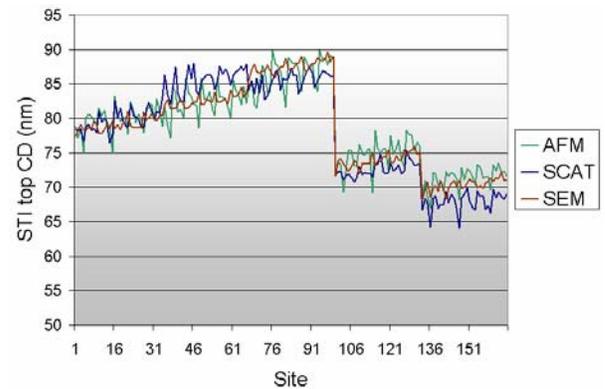


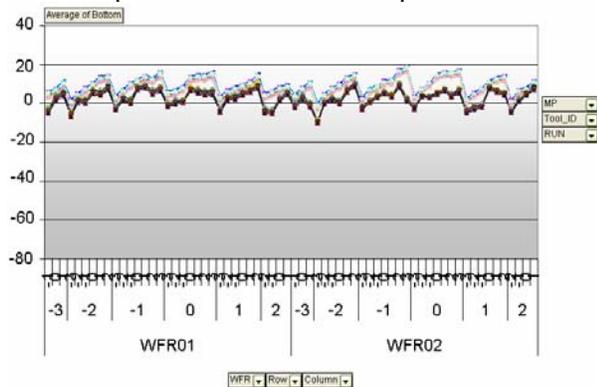
Figure 24. Site-by-site correlation between OS, SEM and reference data for STI top line CD.

Figure 23 presents correlation between SEM and the same set of STI line CD reference data for the 190 nm pitch structure. SEM shows a comparable correlation of 0.92, but a better slope of 0.98. The SEM fleet bias is a minor -0.3 nm. Single tool and fleet precisions are 2.1 nm ( $3\sigma$ ) and 2.2 nm ( $3\sigma$ ), respectively. The fleet TMU is estimated to be 5.75 nm ( $3\sigma$ ). Although, OS and SEM fleet TMU values are close, the discrepancy with the reference data seems to be different as follows from Figures 22 and 23. Figure 24 presents a site-by-site correlation between OS, SEM and reference data. While the OS data shows better across wafer correlation but variable wafer-to-wafer bias to the reference data, the SEM data seems to show better wafer-to-wafer correlation but less sensitivity to across wafer STI line CD variation. The estimates for both OS and SEM fleet TMUs of STI line CD measurement are disturbingly high. Analysis of the root cause of the high TMU of the SEM fleet is beyond the scope of this paper. In cases of marginal metrology, the simultaneous use of more than one CD process control technique helps reduce the risk of operation with high TMU.

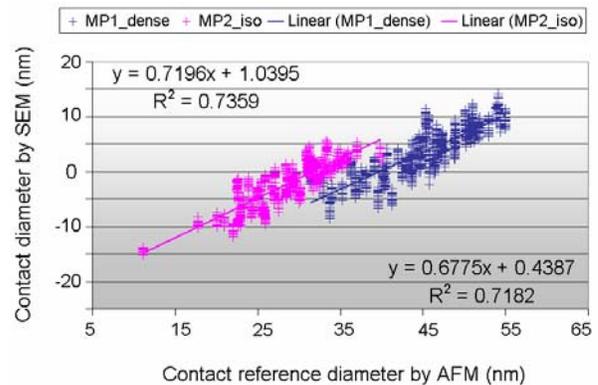
### 3.5. Contact CD metrology

Contact and via metrology is arguably the most challenging CD metrology of the 65 nm technology. Complex sidewall profile and hole roughness could easily obscure CD metrology (Fig. 10). Comprehensive CD SEM measurement algorithms, which include averaging CDs of several holes, were designed and implemented to deal with this problem. In this MSA an attempt was made to estimate the TMU and accuracy of CD SEM contact diameter measurements. Two FEM contact post etching wafers were used in the study. The total number of calibrated sites was 132 (66 dense with pitch 200 nm and 66 isolated sites). Figure 25 shows dense and isolated contact CDs by site as measured more than seven days by two baseline CD SEM tools. Figure 26 presents the correlation between SEM and reference contact diameter data. The dense contact data shows a correlation of 0.85 and a slope of 0.68. The fleet TMU was estimated as 3.7 nm ( $3\sigma$ ) using uncertainty of the reference data of 5.1 nm ( $3\sigma$ ). Single tool and fleet precisions were 3.2 nm ( $3\sigma$ ) and 3.3 nm ( $3\sigma$ ), respectively. The isolated contact data indicated a correlation of 0.86 and a slope of 0.72. The fleet TMU was estimated as 4.3 nm ( $3\sigma$ ) using uncertainty of reference data of 3.3 nm ( $3\sigma$ ). A single tool and fleet precisions were 2.1 nm ( $3\sigma$ ) and 2.2 nm ( $3\sigma$ ), respectively. For both dense and isolated contacts, single tool precision contributes noticeably to the fleet TMU. Data shows that the SEM contact diameter changed systematically during the MSA (Fig. 27). Contact site charging could explain the reported diameter drift. As anticipated, charging an isolated hole and array of holes may have different amplitude and dynamics. It is worth noting that dense and isolated contacts show a different range and dynamic of the diameter drift (Fig. 27).

The trend (or drift) correction of SEM data was not used in this MSA. Therefore, the values reported for precision and TMU are most likely overestimated. A new data collection and evaluation procedure, which includes data trend correction, was developed for a fleet of unlimited number of metrology tools [14]. The procedure was not available at the time of the MSA. Based on data available today it is estimated that after trend removal the SEM fleet TMU for dense contact CD measurements should be  $\sim 2.1$  nm ( $3\sigma$ ). The TMU for isolated contact CD measurements would need further improvement to meet an acceptance criterion.



**Figure 25.** Dense and isolated contact CDs by SEM fleet.



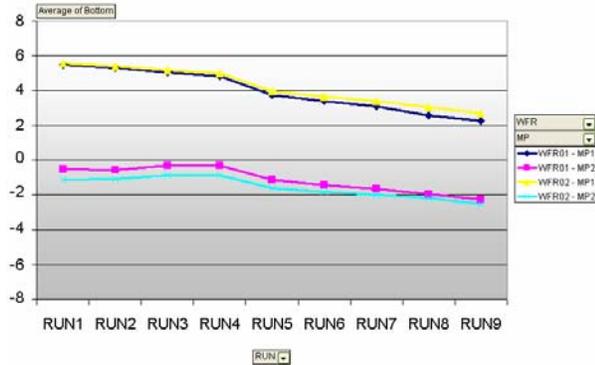
**Figure 26.** The correlation between SEM and reference CD data for dense and isolated contacts.

The reference contact diameter data were taken at 130 nm from the very top of pre-metal dielectric layer. As Figure 26 shows, the reference “top” contact diameter measured by CD AFM is noticeably larger than the “bottom” contact diameter reported by CD SEM (Fig. 32). The depth at which CD AFM can reliably measure contact diameter was limited by the length and stiffness of 50 nm AFM probes. Sixteen TEM images were used to estimate bias between the reference contact diameter measured at 130 nm and the true bottom diameter of the contact. CD AFM has  $(36.9 \pm 2.3)$  nm and  $(30.5 \pm 4.0)$  nm diameter bias for dense and isolated contacts, respectively. The uncertainties are reported for CL of 0.95. After the TEM based correction was applied to the CD AFM data, the SEM fleet bias for the dense contacts was estimated as -4.5 nm. The SEM fleet bias for the isolated contact diameter was -0.3 nm. Once again, the CD AFM hole diameter measurements are untraceable to the NIST standards. Therefore, the reported fleet biases, as well as correlation and slope values, are our best possible estimates.

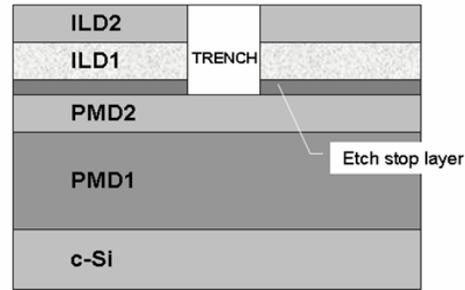
### 3.6. Interconnect trench CD metrology

The back end of line (BEOL) CD metrology is another critical part of semiconductor technology often unjustifiably neglected. Historically, BEOL technology relied on direct electrical CD control. Special electrical test structures are widely used for interconnect trench CD measurements. Trench CDs today are as small as 65 nm. The trench aspect ratio

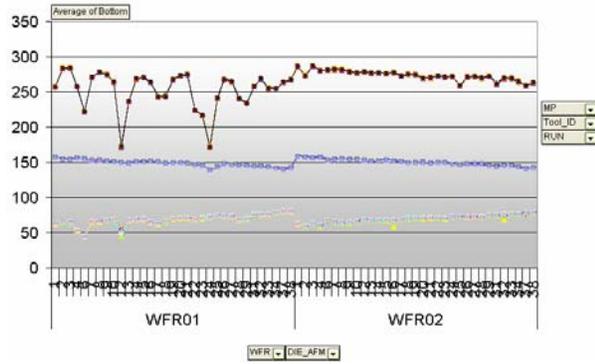
reaches 4. Special barrier layers are used to isolate metal line from interlayer dielectrics (ILD). Under such circumstances many original assumptions used to calculate trench CDs based on electrical data simply do not work. Accuracy and TMU of electrically based CD metrology are questionable. This leads to the importance of OS and SEM based interconnect CD metrologies. The TMU of BEOL CD metrology, as with the gate or STI metrologies, is impacted by time, tool and sample dependent measurement bias variations. Therefore, similar MSA protocols were used for BEOL CD metrology evaluation.



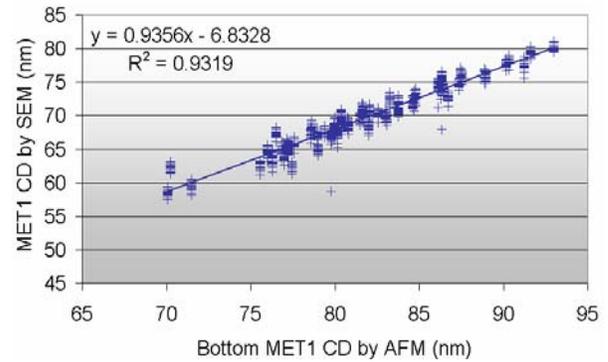
**Figure 27.** Dense and isolated contact diameter time trends.



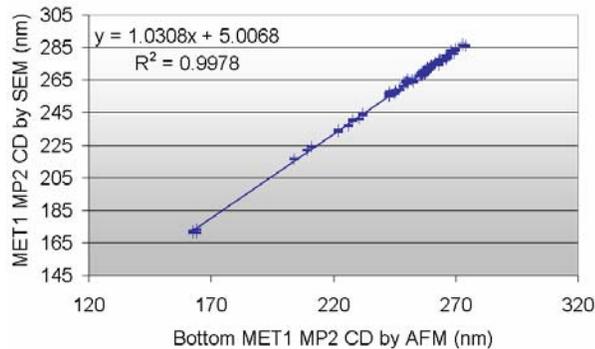
**Figure 28.** Interconnect stack and MET1 trench geometry.



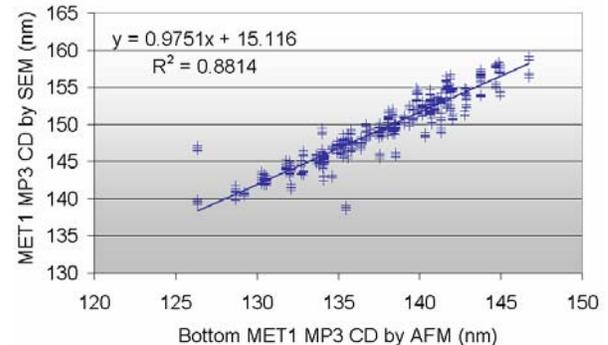
**Figure 29.** MET1 trench CDs as measured by SEM fleet.



**Figure 30.** The correlation between SEM and reference data for MET1 MP1 trench CD.



**Figure 31.** The correlation between SEM and reference data for MET1 MP2 trench CD.



**Figure 32.** The correlation between SEM and reference data for MET1 MP3 trench CD.

Complex MET1 interconnect stack and trench geometry are illustrated in Figure 28. Three parameters are normally used to characterize the trench: CD, depth and SWA [1]. The MSA is focused on MET1 trench CD SEM metrology. One EM and one FEM wafers with a total of 210 pre-calibrated sites were used for the MSA. The following structures (features) were measured for more than seven days on three baseline tools: MP1 = 180 nm pitch (90 nm trench), MP2 = 450 nm pitch (230 nm line) and MP3 = 280 nm pitch (100 nm line). Figure 29 shows trench CDs by site for all SEM tools and repeats. Figures 30-32 present the correlations between SEM and reference data for trench and line bottom

CDs of the interconnect structures. All three dependencies show a very good correlation of 0.97, 1.00 and 0.94; a slope of 0.94, 1.03 and 0.98; and fleet bias of -12.0 nm, 12.7 nm and 11.7 nm, respectively. The change of sign of SEM bias is expected since MP1 is a trench and MP2 and MP3 are lines. The SEM also demonstrates acceptable single tool precisions of 2.1 nm ( $3\sigma$ ), 1.3 nm ( $3\sigma$ ) and 1.1 nm ( $3\sigma$ ), respectively. Corresponding SEM fleet precisions are 2.4 nm ( $3\sigma$ ), 1.5 nm ( $3\sigma$ ) and 1.3 nm ( $3\sigma$ ), respectively. The SEM fleet TMU is estimated to be 3.2 nm ( $3\sigma$ ), 2.3 nm ( $3\sigma$ ) and 3.4 nm ( $3\sigma$ ) for MP1, MP2 and MP3, respectively. In all three cases the TMU/T ratio is less or close (MP1) to the acceptable level of 0.2.

#### 4. DISCUSSION

The MSA results reported in section 3 are summarized in Table 1. Metrology bias, TMU and precision are reported in nanometers. SWA values are in degrees. Process tolerances are estimated as 10% ( $3\sigma$ ) of the controlled value for STI and gate and 15% ( $3\sigma$ ) for interconnect trench dimensions [15]. For gate SWA a tolerance of  $1^\circ$  has been used [1].

Despite a few detected problems overall status of 65 nm CD metrology is acceptable. As expected OS metrologies have better precision and smaller bias. CD SEM correlates well with reference data and has good linearity. Contact CD SEM metrology is marginal but most likely will be improved once CD trends are removed and uncertainty of reference data is improved. The establishment of hole CD metrology accuracy is a challenge.

**TABLE 1.** Summary table.

METROLOGY	BIAS	FLEET TMU	CORREL	SLOPE	FLEET PRECISION	PRECISION	TMU/T
Gate CD OS	-0.2	0.8	0.99	1.05	0.7	0.5	$\leq 0.2$
Gate SWA OS	-1.0	0.8	0.70	0.84	0.5	0.2	$> 0.2$
Gate CD SEM	8.8	2.3	0.98	1.01	2.3	1.6	$> 0.2$
Gate LDD spacer OS	-2.8	0.7	0.93	0.80	0.4	0.3	$\leq 0.2$
Gate HDD spacer SEM	14.2	2.1	0.99	0.99	2.0	1.3	$\leq 0.2$
STI line CD OS	-0.8	5.7	0.93	1.16	1.2	0.5	$> 0.2$
STI line CD SEM	-0.3	5.8	0.92	0.98	2.2	2.1	$> 0.2$
Contact CD SEM (dense)	-4.5	3.7	0.85	0.68	3.3	3.2	$> 0.2$
Contact CD SEM (iso)	-0.3	4.3	0.86	0.72	2.2	2.1	$> 0.2$
Trench CD SEM MP1 (space)	-12.0	3.2	0.97	0.94	2.4	2.1	$> 0.2$
Trench CD SEM MP2 (line)	12.7	2.3	1.00	1.03	1.5	1.3	$\leq 0.2$
Trench CD SEM MP3 (line)	11.7	3.4	0.94	0.98	1.3	1.1	$\leq 0.2$

A problem with gate SWA metrology is detected. The lack of a universal definition of gate SWA and the NIST traceable SWA standards contributes to the problem. The SWA measured by CD AFM is scanning parameters and probe sharpness dependent. Better SWA reference metrology is needed.

STI CD metrology is a challenge for both OS and SEM. The STI post etching stack and trench geometry are complex. Sample-to-sample bias variation is significant for both OS and SEM STI CD metrologies. Both techniques need improvement. It seems that OS has a better chance to separate different cross-correlating parameters and extract true STI CD from the complex signal. Although OS must be improved to do that.

#### 5. CONCLUSION AND FUTURE WORK

A new MSA methodology has been developed at TI to evaluate the status of the 65 nm technology CD metrology and its readiness for production. At every critical process level precision, bias, linearity and the TMU were evaluated for complete metrology fleet over an extended period of time. The technology representative set of test samples with CD variations covering process space were pre-calibrated using CD AFM. Precision of the CD AFM measurements was determined for every analyzed process level based on repeated measurements conducted over several days. The NIST traceable standards were used to verify CD AFM line CD and XYZ scale calibrations. The NIST traceability was established for CD metrology at every critical process level for the entire technology. The MSA indicates an overall healthy status of the 65 nm CD metrology. Sub-nanometer accuracy has been established for gate and gate LDD spacer CD metrologies. The thorough MSA and specifically absolute CD metrology calibration were instrumental in early technology qualification and the seamless transfer from 200 mm to 300 mm fabs.

The MSA also revealed several CD metrology problems and challenges. Most of the problems were known from previous studies [1, 5]. SEM has a systematic problem with bias of CD measurements. The problem is common for front-end and back-end of line process levels. For most process levels TMU and precision of CD SEM are noticeably affected by sample modification inflicted by electron irradiation (shrinkage, charging, buildups, etc.). The sample instability causes difficulty, especially in the case of fleet TMU evaluation. An improved data collection methodology was devised to minimize the impact of sample instability on fleet TMU measurements [14]. The advanced procedure will be used on future CD metrology MSA.

Some systematic problems were detected with CD OS. This study confirms observations made a year ago [1]. Most OS models had persistent problem with TMU, which revealed itself through poor data linearity. Cross-correlation between parameters of OS models is a common problem. Performance of CD OS for the 65 nm technology is acceptable, but marginal. Despite recent optimistic forecasts [16,17] noticeable OS problems are expected for 45 and 32 nm technology nodes. Simple estimates show that the OS signal is cut almost in half with each sequential technology node because of constant reduction of line CD, height and OS target size. It is a common practice to estimate limits of OS sensitivity based on the noise of the OS system [18]. In reality, so-called “process” noise, or noise caused by uncontrolled and not included in the OS model process variations, exceeds OS’ own noise. Once OS signal-to-noise ratio reaches a “grey” area the cross-correlation of OS model parameters becomes dangerous and may damage OS TMU and accuracy. Based on the 65 nm technology experience, we encourage OS suppliers look again at OS sensitivity limits and try to develop more robust CD OS solutions for technologies to come.

Accurate reference data is a key for detection and to solve the CD metrology problems. We believe that accurate CD metrology is required for modern technology development. For the last two to three technology nodes, CD AFM was used as a reference metrology. We hope that this article and other papers published at the conference will attract attention to these questions: What are the challenges of modern CD AFM? What are alternative reference CD metrologies? Do we have reliable reference CD metrology to support future technology development? Who is working on the future reference CD metrology?

Solving these complex CD metrology problems will require collective effort of many semiconductor companies and scientific institutions. As an example, this work became possible after a recent breakthrough in line CD standard technology [2, 3], recognition of CD AFM as an instrument for CD traceability [4,5] and development of the concept and mathematical tools for TMU analysis [6,7].

## 6. ACKNOWLEDGMENTS

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- <sup>6</sup> J. Mandel, *The Statistical Analysis of Experimental Data*, Interscience Publishers, John Wiley & Sons, NY, 1964.
- <sup>7</sup> B. Banke and C. Archie, “Characteristics of accuracy for CD metrology,” SPIE Proceedings, Vol. 3677, 291-308 (1999).
- <sup>8</sup> The TMU as defined in Figure 1 is not truly a random error. Sample-to-sample and tool-to-tool components of the TMU are not necessarily random or normally distributed. However, if a single tool precision is a dominating component of TMU such approximation may not be too far from reality.
- <sup>9</sup> It is understood that it is virtually impossible to represent the entire process space with a limited number of wafers fabricated in limited period of time. Therefore, the complete and final evaluation of CD metrology can be done with

systematic in-line accuracy checks conducted over extended period of time. The in-line CD metrology evaluation is beyond the scope of this article. The MSA methodology reported in the article is design with an intention to mimic the in-line testing as close as possible and to provide fair estimates of metrology fleet characteristics.

<sup>10</sup> To make the estimate we assumed that both the top and the bottom CD vary independently by  $\pm 0.6$  nm and that line height of 100 nm varies less than  $\pm 2$  nm.

<sup>11</sup> Microsoft Excel SLOPE function was used to evaluate linearity (slope) of fleet under evaluation data.

<sup>12</sup> Microsoft Excel CORREL function was used to calculate correlation between of fleet under evaluation and reference data.

<sup>13</sup> J. Mandel, "Fitting straight lines when both variables are subject to error," *Journal of Quality Technology*, pp. 1-13, January 1984. J. Mandel, *The statistical analysis of experimental data*, Interscience Publishers, John Wiley & Sons, NY, 1964.

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